Ministère de l'Enseignement Supérieur
et de la Recherche Scientifique
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وزارة التعليم العالي والبحث
العلمي
جامعة 20 أوت 1955 – سكيكدة

Practical Works

OF SEMICONDUCTORS

01 *Hall Effect*

02 *PN Junction*

03 *MOS Capacitors*

04 *MOS transistors*

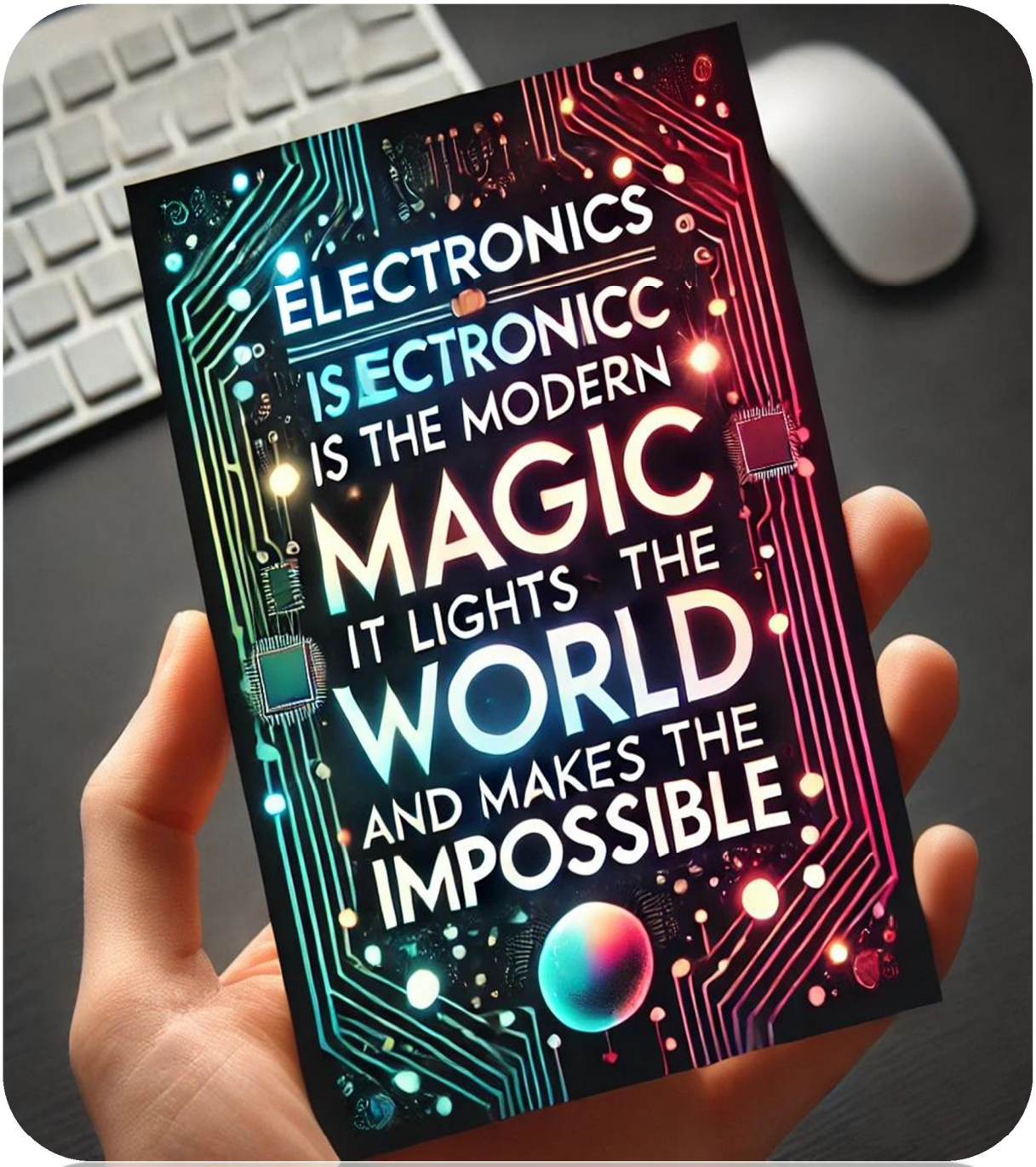
05 *Diode junction applications*

L3 *Physics of materials*

By

Dr. GACEM Amel

2024 - 2025


ELECTRONICS
IS ECTRONICC
IS THE MODERN
MAGIC
IT LIGHTS THE
WORLD
AND MAKES THE
IMPOSSIBLE

L'équipe pédagogique peut rajouter (ou remplacer) certains manips selon le matériel disponible.

UEM23 / M233

TP physique des semi-conducteurs

(1h30' TP/ semaine) ; 22h30'/Semestre

Crédits : 02 Coefficient : 01

Objectifs de l'enseignement : On réalise quelques manipulations pour comprendre et maîtrise quelques phénomènes spécifiques de la physique des semi-conducteurs.

Connaissances préalables recommandées : Semi-conducteurs, physique de solide.

Contenu de la matière :

- Effet Hall.
- Jonction PN.
- Capacité MOS.
- Transistor MOS.
- Applications des diodes à jonction PN.

Mode d'évaluation : Compte rendu : 50% Examen : 50%

Références (Livres et polycopiés, sites internet, etc)

1. A. Vapaille et R. Castagné "Dispositifs et circuits intégrés semiconducteurs", Dunod.
2. Ashcroft et Mermin "Physique des solides".
3. Mathieu et Fanet " Physique des semi-conducteurs et des composants électroniques".

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Foreword

This manuscript of Practical Works of semiconductor module is dedicated to the third year students license (L3) Physics of materials. It's in accordance with the official program.. Any student taking a semiconductor course can also use it profitably. It contains the description of five practical work (5PWs) through which, the student should verify and deepen his theoretical knowledge on the one hand and acquire experimental know-how on the other hand, and this in a field as exciting as that of materials and in particular semiconductors.

All of this practical work can be carried out with simple means that any measurement laboratory has. The results obtained are comparable to those from experiments using specialized and expensive equipment. Each experiment described has 3 parts: the aim of the manipulation which defines the objectives in a clear, precise and quantifiable way, a theoretical part which consists of a theoretical reminder of the subject of the experiment and a practical part in which the operating mode is described. The objective of this brochure is to provide a support of practical work while aiming for a better exploitation of the teaching material available at the level of our department of physics. This handout contains five practical works that will allow students to better understand, assimilate, deepen, and visualize or highlight the practical side of certain theoretical notions learning during the sessions of the courses and the tutorials.

Content of subject:

1. *Hall effect.*
2. *PN junction.*
3. *MOS capacitance.*
4. *MOS transistor.*
5. *Applications of PN junction diodes.*

I wish all our students a very good university course and a path full of success.

Dr. GACEM Amel

Tips on the conduct of the experiment

During the manipulations, precautions must be taken:

- Safety: it is important before any manipulation to check that all the devices are not powered (the equipment in off mode).
- Before starting the measurements, first let the Professor responsible for practical work check the assembly.
- Always check the calibres of the measuring devices.
- To plot the curves, it is mandatory to use the computer tool (use of Origin software or others such as Excel).

At the end of each experiment, a report must be written.

This report contains:

- A cover page, which bears the name of the student, the PW number, the title of the experiment and the current year. - A short introduction where the student indicates the purpose of the manipulation.
- A theoretical description,
- The answer to the questions asked.
- A conclusion that summarizes/discusses the results obtained.

Quantities and Units in Electronics

a) Quantities

The first table shows electrical quantities, which are used in electronics. The relationship between quantities can be written using words or symbols (letters), but symbols are normally used because they are much shorter.

Quantity	Usual Symbol	Unit	Unit Symbol
Voltage	V	volt	V
Current	I	amp*	A
Charge	Q	coulomb	C
Resistance	R	ohm	Ω
Capacitance	C	farad	F
Inductance	L	henry	H
Reactance	X	ohm	Ω
Impedance	Z	ohm	Ω
Power	P	watt	W
Energy	E	joule	J
Time	t	second	s
Frequency	f	hertz	Hz

* strictly the unit is ampere, but this is almost always shortened to amp.

b) Units

The second table shows the unit (and unit symbol) which is used to measure each quantity. For example: Charge is measured in coulombs and the symbol for a coulomb is C. Some of the units have a convenient size for electronics, but most are either too large or too

small to be used directly so they are used with the prefixes shown in the second table. The prefixes make the unit larger or smaller by the value shown.

Prefix	Prefix Symbol	Value	
milli	m	10^{-3}	= 0.001
micro	μ	10^{-6}	= 0.000 001
nano	n	10^{-9}	= 0.000 000 001
pico	p	10^{-12}	= 0.000 000 000 001
kilo	k	10^{3}	= 1000
mega	M	10^{6}	= 1000 000
giga	G	10^{9}	= 1000 000 000
tera	T	10^{12}	= 1000 000 000 000

Example:

25 mA = 25 × 10^{-3} A = 25 × 0.001 A = 0.025 A

47μF = 47 × 10^{-6} F = 47 × 0.000 001 F = 0.000 047 F

270 kΩ = 270 × 10^{3} Ω = 270 × 1000 Ω = 270 000 Ω

Why not change the units to be better sizes?

It might seem a good idea to make the farad (F) much smaller to avoid having to use μF, nF and pF, but if we did this most of the equations in electronics would have to have factors of 1000000 or more included as well as the quantities. Overall, it is much better to have the units with their present sizes, which are defined logically from the equations. In fact, if you use an equation frequently you can use special sets of prefixed units, which are more convenient...

Example:

Ohm's Law: **V = R I**

The standard units are volt (V), amp (A) and ohm (Ω), but you could use volt (V), milliamp (mA) and kilo-ohm (kΩ) if you prefer. Take care though; you must never mix sets of units: using V, A and kΩ in Ohm's Law would give you wrong values.

Contents Table

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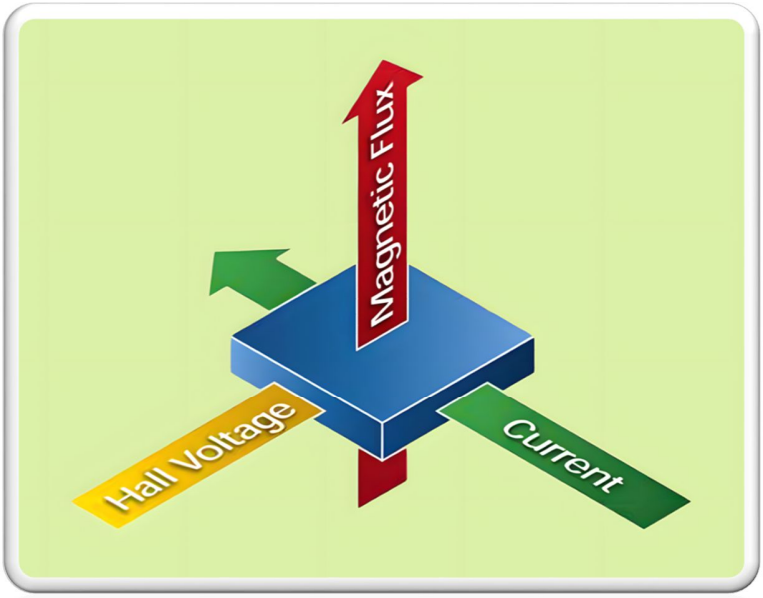
Practical Works 01

Hall Effect

L3 physics of materials



By Dr. GACEM Amel

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Hall Effect Theatrical Section

1. Introduction

The Hall Effect is a physic phenomenon produced when electrical current flows through a metallic or semi-conducting material subjected to a magnetic field perpendicular to the current. The Hall Effect states that a static magnetic field produces a potential difference perpendicular to the plane of current flow and magnetic field. This voltage is called Hall voltage and is proportional to the current and magnetic field strength and has a wide range of applications such as Hall Effect sensors, Hall Effect current meters, Hall Effect switches etc. The Hall Effect has become increasingly important in modern technology. For example, applications in solid state devices are discussed as well as the high temperature superconductors, nano-sized materials and other two-dimensional materials systems. Hall Effect measurements can also provide information on the density and type of majority charge carriers, their drift mobility and the conductivity of the material, which can be useful for characterizing transistors, semiconductors and dies. A detailed study of Hall Effect in metals and semiconductors is done using a simple experimental set-up. A magnetic field is applied perpendicular to the plane of metal or semiconductor and the Hall voltage is measured across it. Given a constant current, the Hall voltage is proportional to the applied magnetic field.

2. Definition

The Hall effect is the deflection of electrons (holes) in an n type (p type) semiconductor with current flowing perpendicular to a magnetic field. The deflection of these charged carriers sets up a voltage, called the Hall voltage, whose polarity depends on the effective charge of the carrier. The Hall Effect refers to the generation of voltage across a conductor when it is placed in a magnetic field that is perpendicular to the direction of current flow. This arrangement creates a force perpendicular to both the magnetic field and the current, resulting in charge carriers accumulating on one side of the conductor, thereby generating a voltage difference, known as Hall voltage. In the 1940, the Hall Effect found a niche in semiconductor research. Here, Hall measurements provided a way to determine the type of majority carrier and its density. In the mid-1950, the technology matured to the point that commercial devices were sold, marking the

Hall Effect's transformation from a laboratory curiosity to a practical tool. In the 1970, Hall Effect devices transformed from discrete components to integrated circuit form. By the 1990, large-scale integration meant multiple Hall Effect sensors could be placed on the same die as the supporting electronics, making them suitable for high-volume applications like automotive use. Seven decades after its discovery, the Hall Effect found its most important application in the automotive industry. In the late 1950, onwards, the enduring legacy of Hall's effect continues to inspire a higher level of research interest in any newly discovered similar effects conceivable.

3. Basic Principles

The underlying principles of Hall Effect are examined at the core of the Hall Effect. It expands on how charged particles behave in a magnetic field and how these principles helped develop the Hall phenomenon. It continues to explain how electric current and magnetic fields interact through physics constructs that everyone has come across in their studies. These include Lorentz force and its equation. In addition, it emphasizes how materials contain charge carriers and how these charge carriers make Hall Effect appear within materials. It goes on to explore how charge density and mobility are defined in a material and how these two fundamental parameters influence observable outcomes in experiments. Mobility is discussed further with Hall Effect considerers Number and the role of Hall Voltage in making practical use of the Hall Effect.

A magnetic field is created whenever there is an electric current, and when a wire carrying electric current is exposed to an external magnetic field, it experiences a force. This phenomenon was well known to physicists before Hall's experiments. The force experienced by a current-carrying wire in a magnetic field was quantized by a physicist named Lorentz. He found that the force on a wire is proportional to both the current in the wire and the magnetic field strength. This explains the fundamental principle behind the usage of current-carrying wires in electric devices such as electric motors and speakers. Concerning the Hall Effect, electric devices are used in magnetics experiments.

4. Mathematical Formulation

The Hall Effect is a phenomenon observed in conductors when they carry current and are placed in a magnetic field. It results in the development of a transverse voltage across the conductor, perpendicular to both the current direction and the magnetic field. The mathematical formulation of this effect is essential for understanding and predicting its behavior quantitatively.

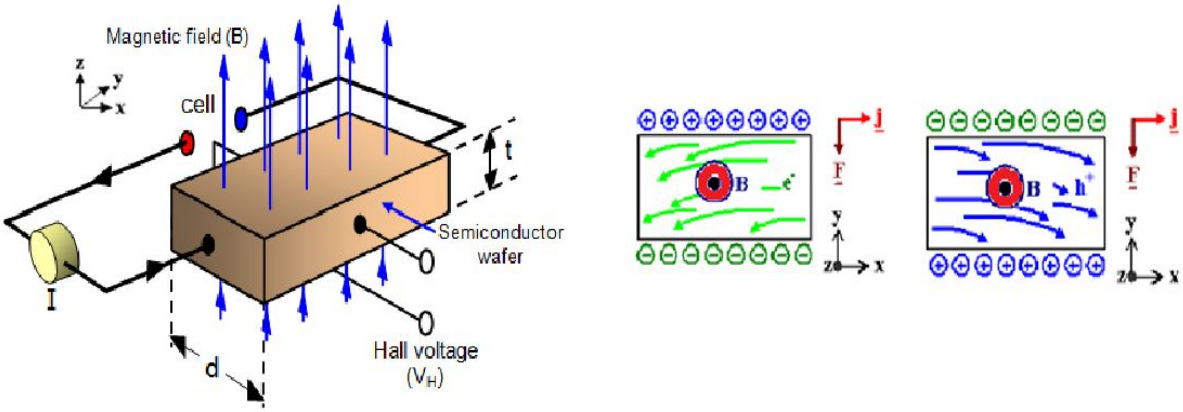

Figure 1 The Hall effect.

The Lorentz Force Equation describes the force experienced by charged particles moving within a magnetic field. It expresses the relationships among electric charge (q), velocity (v), and the magnetic field strength (B), essential for grasping the principles behind the Hall Effect . "The total Lorentz force, F, acting on the charge, q, moving with velocity v in the presence of electromagnetic fields is given by".

$$F = q[E + (v \times B)]$$

Here, E is the electric field, v is the velocity of the charged particle, q is the charge of the particle, and B is the magnetic field. Equation 1 can be simplified. If there are only magnetic fields, the above equation can be expressed as:

$$F = q(v \times B)$$

This Lorentz force causes a drift velocity, v_d, on the charge carrier of Conductors in a magnetic field, given by:

$$v_d = (F/m)$$

The Lorentz force (F) acting on the charge carrier (with mass m) determines the drift velocity.

$$\varphi_d = (q(v \times B)/m)$$

Here, φ_d is the angle between the field-vector v and the magnetic field-vector B. Rearranging leads to:

$$qB = (m\varphi_d)/v_d$$

This result shows the relationships among charge, geometry, and magnetic field strength. It can be used to predict the Hall Effect's behavior in different situations, given the material description. To develop the Hall voltage, V_H, the net current flowing across a rectangular conductor in a magnetic field can be analyzed. The forces acting on the charge carriers in the conductor can be derived using the Lorentz force equation is:

$$F = Bqv_x$$

Here, B is the magnetic field, q is the charge of each charge carrier, and v_x is the velocity of charge carriers along the x-axis (current flow direction), determined by

$$J = nvq$$

Charge carrier density, n, drift velocity, v_x, and conduction current density, J, relationship yield:

$$v_x = J/nq$$

The current density into Equation leads to:

$$F = B(J/n)$$

The electrostatic force, Fe, counterbalances forces acting on each charge carrier as charge redistribution leads to an electric field developing along the y-axis.

$$F_e = qE$$

The Hall voltage develops across a conductor in a magnetic field.

$$\sum F = 0 \rightarrow B(J/n) - qE = 0$$

$$E = (B/n)J$$

If the Hall coefficient, R_H, is defined as:

$$R_H = E_y/(J_zB)$$

Where E_x is the Hall voltage and w is the width, the Hall voltage can be derived as:

$$E_y = (1/n)J_zB$$

$$E_x = (E_yw) = (wB/n)J_z$$

In this equation, the Hall coefficient displays the Hall Effect's dependence on material:

- ✓ For metals, n is negative, making R_H negative.
- ✓ On the other hand, for semiconductors, p is positive, making R_H positive.

The Hall coefficient can be used to determine the mobility of the charge carriers:

$$\mu = R_H\,\sigma$$

Where σ is conductivity of the material.

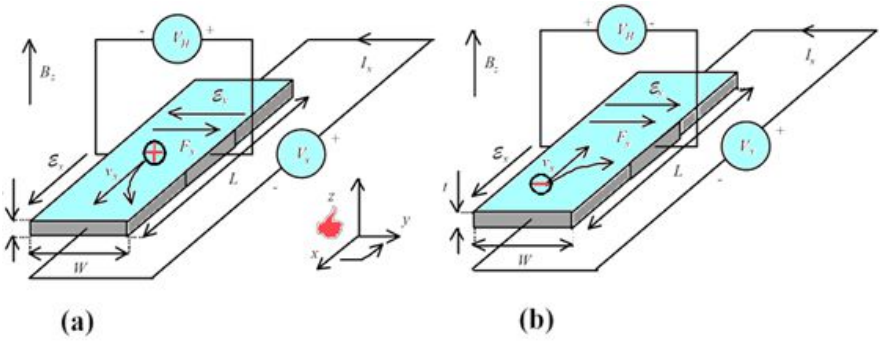

Figure 2 Hall setup and carrier motion for a) holes and b) electrons.

As shown in Figure 2(a), the holes move in the positive *x*-direction. The magnetic field causes a force to act on the mobile particles in a direction dictated by the right hand rule. As a result there is a force, F_y, along the positive *y*-direction, which moves the holes to the right. In steady state this force is balanced by an electric field, E_y, so that there is no net force on the holes. As a result there is a voltage across the sample, which can be measured with a high impedance voltmeter. This voltage, V_H, is called the Hall voltage. Given the sign convention as shown in Figure 2(b), the hall voltage is positive for holes.

5. Experimental Setup and Procedure

This section presents the necessary equipment and materials needed to conduct experiments associated with the Hall Effect. These items are detailed to a sufficient extent that, by ensuring these materials, the experimental setups can be replicated effectively. This preparation means that readers are fully prepared to engage with the practical work exploring the Hall Effect. The procedure for the experiments is also detailed on a step-by-step basis, guiding users through the important stages of the work from initial experimental setup through to the collection of results. These details include the procedures which need to be followed, the things that need to be considered, and the precautions that need to be taken. In particular, the need for attention to safety and accuracy is highlighted, as is the importance of careful planning to ensure that experimentation is both reliable and effective.

Finally, the importance of taking into consideration the variable factors which could affect the results during the experimental phase is discussed. In light of the potential for variation in the results obtained to limit their significance, readers are encouraged to adopt a systematic approach in their own experimental design that will control the variability of the factors affecting the results and allow significant findings to be yielded. Rather than providing a cookbook for practical work with the Hall Effect, this section aims to provide sufficient information that practical experiments can be carried out successfully while also encouraging readers to think critically about their own .

This section provides a straightforward protocol for carrying out experiments on the Hall effect that can be used by advanced undergraduates and beyond in laboratory classes, as the techniques are reasonably easy to implement. Experimenters are advised to have a good working knowledge of voltage and current measurement techniques, as well as familiarity with the operation of the equipment specified below. The details can be readily adapted if other equipment and materials are available, especially in regard to the width and thickness of the Hall effect sample. Users are also encouraged to consider the sample preparation outcomes (e.g. size, shape, mounting, ohmic contact configuration etc.) before reading the steps. Hall effect samples are generally thin conductors, on the order of a few hundred micrometers thick. For thin samples, voltages must be interpreted with care. Apparatus needed includes a Hall effect sample, DC power supplies, an ammeter, voltmeters, multi-meters, a digital Gauss meter, an oscilloscope with differential probes, etc.

Step 1: Setup Equipment

* Assemble the apparatus so that the magnetic field sensor is either: (A) perpendicular to the planar Hall effect sample, or (B) between the two Hall effect samples, one at room temperature and

the other in the dewar. Use method A for the planar Hall effect and method B for the temperature dependent Hall effect.

* Connect voltmeters and ammeters to data logging software (if desired), making sure the settings are switched to read voltage or current as appropriate.

* Measure the dimensions of the Hall effect sample. Measure the length, width, and thickness at multiple points, recording the averages. The width/length ratio should be noted for the Hall Effect test.

* Set DC current to 0A, and ensure that all other powers are off. For temperature dependent experiments, put the second planar Hall Effect sample in the Dewar.

Step 2: Hall Effect Measurement

* Turn on the power supplies, multimeters, monitor, and computer in that order.

* Execute data logging software and check the setup with a non-zero current input.

* Measure the magnetic field at 0 A, then apply -I A and measure again, repeating until 4 non-zero currents are measured. Measure 1, 3, and 5 A again and check the data agrees with the expectation of symmetry.

* Examine the output graphs, and compare the results to the class notes.

* Measure the resistivity of the sample by applying -I A between the voltage contacts while measuring the Hall voltage V_x. Measure V_x at 0 A, then net 1, 2, and 4 applying +I between the current contacts and measuring V, recording each voltage. Repeat the measurements but apply current to contacts (1 - 2, 3 - 4 should be V_x). Measure 0 A and fit the data to a polynomial for later subtraction.

Step 3: Collect

* For each set of measurements, record the dataset number, temperatures, dimensions of the sample, and material

* Each dataset should contain 4 measurements, noting current and averaging/reading voltages as necessary. For temperature dependent measurements, note hold time and/or cooling procedure.

Step 4: Calculations

* Use collected measurements to calculate the Hall coefficient, charge carrier density, and mobility of the sample.

* If temperature dependent measurements were conducted, consider determining alpha, the temperature coefficient of resistivity, using linear regression.

* Consider using differential probes to apply a series of small test signals to the data collection setup, measuring the waveforms coming back from the voltmeters and collecting the results in a single spreadsheet, greatly simplifying the final step of gaining results.

6. Data Analysis and Interpretation

This section describes how the data obtained from the experiments are processed and interpreted to extract useful results. Several measurements either to test principle applications of the Hall Effect are, or can be performed as part of practical work. In practical work on the Hall Effect, results are generally represented as graphs of Hall voltage against current, usually with a straight line fitted to the data points.

However, straight line graphs can also be regarded as a way of presenting data in reduced form, since the gradient or slope of the line is treated as a calculated result.

As such, it is essential that the data is represented in this way, and care must be taken in ensuring that straight lines are fitted to the data points correctly. When data is represented graphically, it is much easier to see trends in the data and to draw conclusions from it.

The Hall coefficient is an important quantity calculated from experimental results, and it is also desirable to represent this parameter graphically. Data can also be represented in table form, which may be useful in some circumstances, but it is less effective than graphical representation for spotting trends.

Typically measured results are compared to theoretical predictions to ensure that the data has been interpreted correctly, and the method of quantifying agreement between measured and theoretical results is described.

Interpretation of results is generally straightforward, the key task being to decide on the significance of any irregularities that are observed. Experimental results are most useful only if interpretation is performed, since it is this activity that leads to conclusions being drawn.

7. Interpreting Results

In experiments involving the Hall Effect, it is conventional to plot relevant results on a graph, with one variable plotted against another. Here is explored how key results are affected by several important factors, including temperature, purity, and lattice structure of the material.

These are important in order to contextualize what was found in the experiments. Results that are considered beyond the central four experiments may also be of relevance in understanding the

effect of material properties on the Hall Effect. For experimental work, the graph is an effective visual aid. Spectacular changes in the plotted data can enhance understanding and give a clearer picture of what is going on than a table of raw numbers alone. In addition, a well presented graph can bring out key features of the results, focussing attention on them and leaving obscured less significant points. It is important to remember that simple observations cannot usually speak for themselves; things should be brought together in a more complete way to draw out as many conclusions as possible. This means taking care not just to observe relevant features in the results but also to consider what they might mean. Critical thinking should be applied to each set of results to assess whether they are consistent with supporting evidence that the Hall Effect is taking place, or whether they contradict it.

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PN Junction # Practical Section

1. Instrumentation

Hall Effect control unit, sample holder with rigid base, Hall effect cartridge, Digital Gauss meter, Gauss probe mount, electromagnet, electromagnet power supply, electromagnet connecting cable, AC power code (Figure 1(a)).

2. Principle and Working

When a conductor through which current is flowing, is placed in the magnetic field, a potential difference is generated between two opposite edges of the conductor in the direction mutually perpendicular to both the field and the conductor. This potential developed is Hall voltage & the phenomenon is called Hall effect.

In the present setup, the crystal mount on PCB is placed perpendicular to the pole pieces. Magnetic field is produced by electromagnet operated by 0-16V, 5A power supply. Field intensity measured by gauss meter with radial gauss probe. A constant current is passing through the crystal and hall voltage measured via multimeter (Figure 1(b)).

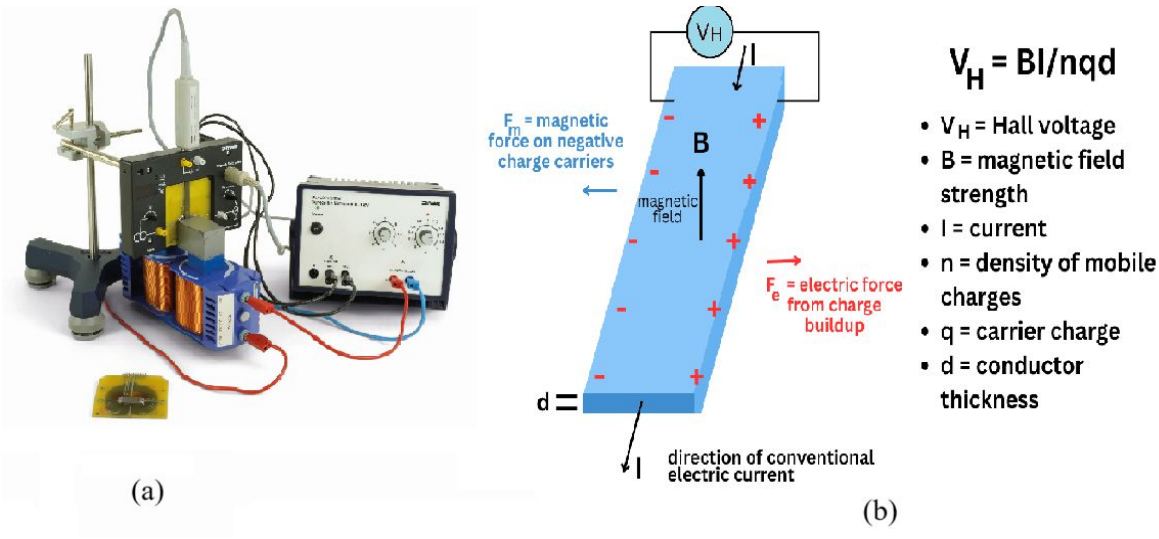


Figure 1 (a) Instrumentation and (b) operating principle.

3. Target of the experiment

The resistivity and Hall voltage of a rectangular germanium sample are measured as a function of temperature and magnetic field. The band spacing, the specific conductivity, the type of charge carrier and the mobility of the charge carriers are determined from the measurements. In this experiment, our Aim is the following: To determine Hall coefficient of semiconductor at room temperature, To measure the carrier concentration of a sample material (Figure 2).

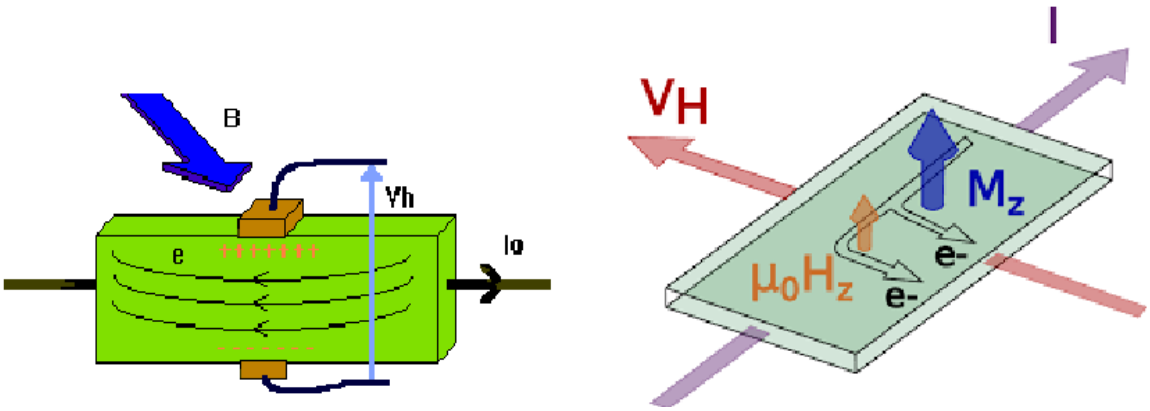


Figure 3 Determine Hall coefficient of semiconductor.

At equilibrium, Lorentz force on a carrier is given by:

$$\vec{F}_m = e(\vec{v_d} \times \vec{B})$$

Drift velocity $\vec{v_d}$ and magnetic field $\vec{B}$ are setup in such a way that they are perpendicular therefore, we can write the above equation as:

$$|F_m| = v_d B$$

Due to accumulation of charges at equilibrium, we develop Hall voltage given by the following relation:

$$|F_H| = e|E_H| = \frac{V_H e}{w}$$

Where w is breadth of above 2D plane as shown above in the figure. $|F_H|$ is the hall force and V_H is the Hall voltage. Now at equilibrium:

$$|F_m| = |F_H|$$

Then we get:

$$v_d = \frac{E_H}{B} = \frac{V_H}{Bw}$$

- **For negative charges:**

If d is the small width of almost 2D plane $d << w < L$. Then the current density of negative charges will be the following:

$$J_L = -nev_d$$

Where 'n' is the concentration of electrons. In addition, we know$I = \vec{J}.\vec{A} = -e.n.w.d.v_d$, we get the following result:

$$V_H = \frac{-IB}{ned}$$

- **For positive charges:**

The results will be similar only the changes will be following:

$$J_L = pev_d$$

Where 'p' is the concentration of holes.

$$V_H = \frac{IB}{ped}$$

We define Hall coefficient as follows:

$$R_H = \frac{E_H}{J_L B} = \frac{V_H d}{IB}$$

Thus:

$$R_H = \frac{1}{ne}$$

4. Results and discussion

a) To measure the Hall voltage as a function of sample current I_H

- **Estimation of Magnetic field:**

Table 1 for current and magnetic field is presented below:

Current (A)	*Magnetic field (Gauss)*
0.01	222
0.25	708
0.50	1273
0.75	1868
1.00	2540
1.25	3190
1.50	3820
1.75	4430
2.00	5010
2.25	5580
2.50	6090
2.75	6540
3.00	6940
3.25	7270
3.50	7560
3.75	7810
4.00	8040

Curve made with Table 1 is illustrated in Figure 4, represented the variation of magnetic field a function of current.

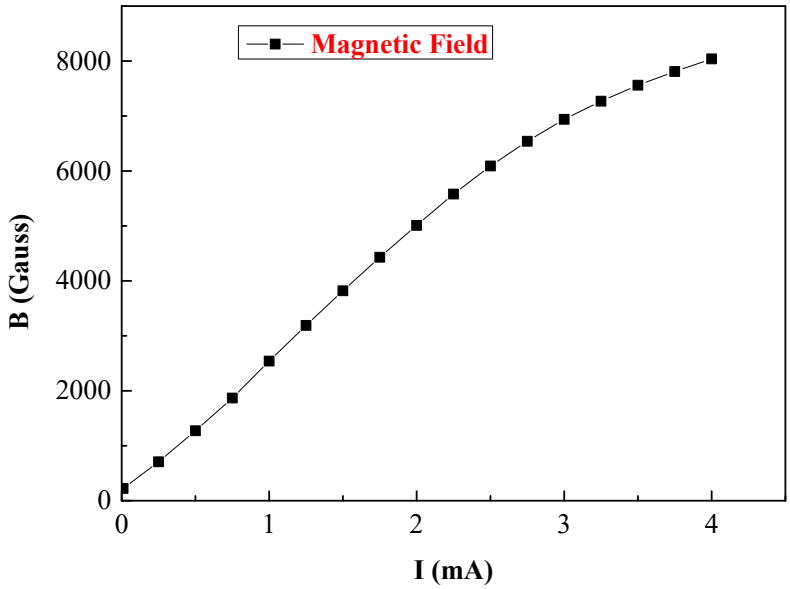


Figure 4 Variation of Magnetic Field a function of sample current.

➢ **<u>The estimation of Hall coefficient for p type Germanium For B = 2540 G:</u>**

The current about the electromagnet: $I_{const} = 1\ A$, the corresponding magnetic field $B = 2540\ G$ (Table 1). Table 2 for current (I) and voltage (V_H) is presented below:

I (mA)	***V_H (mV)***
0.03	0.20
0.58	13.20
1.11	26.20
1.47	34.90
2.00	47.50
2.48	59.00
2.95	70.00
3.57	84.30
4.04	95.00
4.73	110.10
5.29	121.80
5.59	127.60
6.07	136.20
6.60	146.50
6.99	153.10

Curve made with Table 2 is illustrated in Figure 5 presented the variation of Hall voltage a function of current for p type germanium.

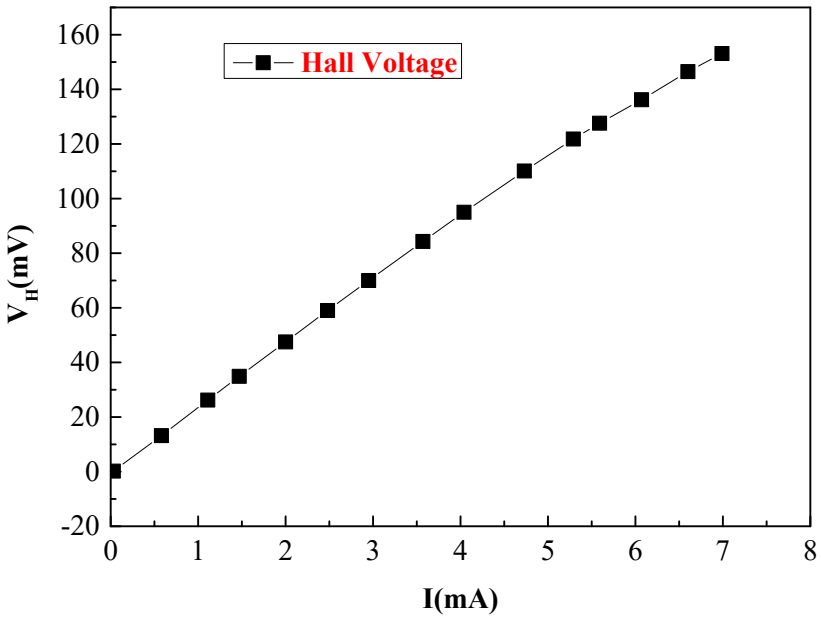


Figure 5 Variation of Hall voltage a function of sample current for p type germanium.

From the above graph: Slop of $V_H(I)$ curve is :

$$Slope = \frac{R_H B}{d} = 22.195\ \Omega$$

Then, for $d = 5 \times 10^{-2} cm$

$$R_H = 43.68 \times 10^3 cm^3 coulomb^{-1}$$

Density of holes: $p = \frac{1}{Re} = 1.43 \times 10^{14}\ cm^{-3}$

Then, the mobility of holes (for σ_p = 0.2 coulomb.volt^{-1}.sec^{-1}.cm^{-1}) is determined by the following relations:

$$\mu_p = R\sigma_p = 8.74 \times 10^3\ cm^2.volt^{-1}.sec^{-1}$$

➢ **The estimation of Hall coefficient for n type Germanium for B = 2540 G** :

The current about the electromagnet: $I_{const} = 1\ A$, The corresponding magnetic field $B = 2540\ G$ (Table 1). Table 3 for current (I) and voltage (V_H) is presented below:

I (mA)	***V_H(mV)***
0.00	0.00
0.45	-4.30
0.92	-9.20
1.56	-15.90
2.03	-20.60
2.43	-24.80
3.06	-31.10
3.57	-36.50
4.02	-41.10
4.55	-46.40
5.08	-51.90
5.50	-56.20
6.01	-61.40
6.50	-66.30
6.99	-71.30
7.50	-76.40

The Figure 6 illustrated the variation of Hall voltage a function of current.

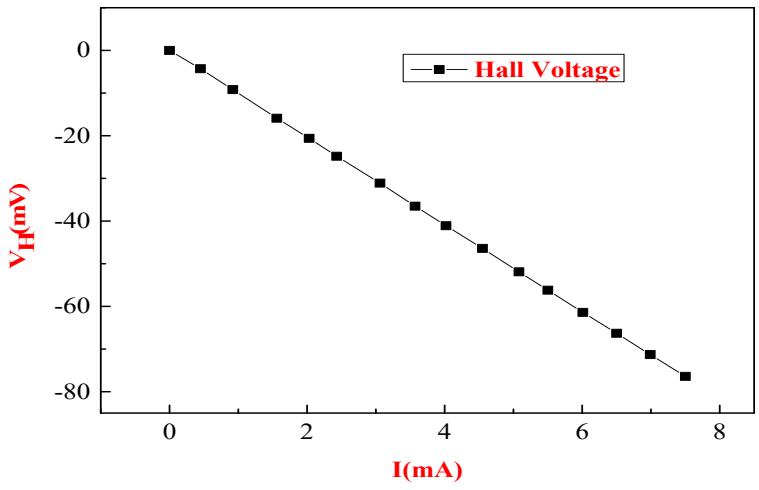


Figure 6 Variation of Hall voltage a function of sample current for n type germanium.

From the above figure: The slope of $V_H(I)$ is determined by the following relationship:

$$Slope = \frac{R_H B}{d} = -10.22\ \Omega$$

Then, for $d = 5 \times 10^{-2} cm$

$$R_H = 20.12 \times 10^3 cm^3 coulomb^{-1}$$

Density of electrons is:

$$n = \frac{1}{Re} = 3.11 \times 10^{14} cm^{-3}\ \ cm^{-3}$$

Then mobility of electrons, for σ_1 = 0.1 coulomb.volt^{-1}.sec^{-1}.cm^{-1} determined by the following formula:

$$\mu_e = R\sigma_e = 2.01 \times 10^3\ cm^2.volt^{-1}.sec^{-1}$$

- ✓ **Error analysis**

Instrumental error

(1) For constant magnetic field, the percentage error in calculating hall co-efficient,

$$\frac{dR}{R} = \left(\frac{dI}{I} + \frac{dV}{V}\right) \times 100$$

Where, dI = least count in probe current measurement = 0.01 mA

dV = least count in hall voltage measurement = 0.1 volt

P type :

$$\frac{dR}{R}\% = \left(\frac{dI}{I} + \frac{dV}{V}\right) \times 100 = 1.9\%$$

N type :

$$\frac{dR}{R}\% = \left(\frac{dI}{I} + \frac{dV}{V}\right) \times 100 = 0.2\%$$

- ✓ **Calculations of Hall coefficients (for constant magnetic field) .**
  - R_H for the p type semiconductor = $43.68 \times 10^3 \pm 0.02\ \ cm^3.coulomb^{-1}$

- R_H for the n type semiconductor = $20.12 \times 10^3 \pm 0.002\ cm^3.coulomb^{-1}$
- Density of holes, p = $\frac{1}{Re} = 1.43 \times 10^{14}\ cm^{-3}$
- Density of electrons, n = $\frac{1}{Re} = 3.11 \times 10^{14}\ cm^{-3}$

For the mobility calculation hall co-efficient is multiplied with conductivity, so error in R will be the error in mobility. So, we have taken the average of errors in R, which will be same with the errors in mobility.

- Mobility of holes is: $\mu_p = R1\sigma_p = 8.74 \times 10^3 \pm 0.009\ cm^2.volt^{-1}.sec^{-1}$
- Mobility of electrons I s: $\mu_e = R2\sigma_e = 2.01 \times 10^3 \pm 0.002\ cm^2.volt^{-1}.sec^{-1}$

Questions / Discussions:

1) **Name one practical use of Hall effect.**

Hall effect is used to determine if a substance is a semiconductor or an insulator. The nature of the charge carriers can be measured.

2) **How is Hall potential developed?**

When a current-carrying conductor is in the presence of a transverse magnetic field, the magnetic field exerts a deflecting force in the direction perpendicular to both magnetic field and drift velocity. This causes charges to shift from one surface to another thus creating a potential difference.

3) **What is a Hall effect sensor?**

A Hall effect sensor is a device that is used to measure the magnitude of a magnetic field.

4) In the Hall effect, the direction of the magnetic field and electric field are parallel to each other. True or False?

False. The magnetic field and electric field are perpendicular to each other.

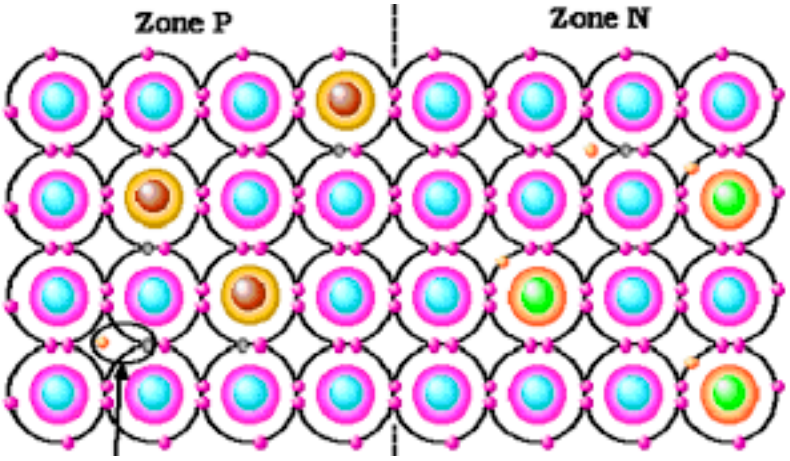
5) **Explain Lorentz Force.**

Lorentz force is the force exerted on a charged particle q moving with velocity v through an electric field E and magnetic field B.

Practical Works 02

PN Junction

L3 physics of materials



By Dr. GACEM Amel

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Theatrical Section

Practical Section

PN Junction Theatrical Section

1. Introduction

A PN junction diode is the most simple form of diode, is a two-terminal device that allows the flow of current in only one direction. Therefore, it is also called a rectifier. This simple diode consists of a junction between p-type and n-type semiconductors. A diode is a basic building block of all electronic circuits. During the forward bias, a diode allows current to flow through it, whereas in reverse bias, it blocks current flow. However, there is a small amount of current that flows even in the reverse direction. This small current is called leakage current and is a two-terminal electronic component that conducts electricity primarily in one direction. it has two terminals: anode and cathode. A diode allows current flow in the forward direction and restricts current flow in the reverse direction. Therefore, it is called a rectifier.

In this practical work, the basic idea, characteristics, and applications of p-n junction diodes are studied in detail. This includes the simple idea of how a diode works and explains the construction and theory of p-n junction diodes. It explains what a p-n junction diode is and how it works. The characteristics of a diode are explained including the current-voltage characteristics in forward and reverse bias, as well as the static and dynamic characteristics of the diode are explained.

2. Definition

PN junction diode is an electronic component that conducts current in one direction only, consists of a piece of semiconductor that is doped with specific impurities to create a P-type and N-type semiconductor that meet. The P-type side has an abundance of holes, while the N-type side has many free electrons. When freshly manufactured, there are no external voltage or current sources connected to the diode (Figure 1). Therefore, the diodes are said to be in equilibrium conditions, as charge carriers diffuse from one region to another, they slowly fill the depletion region, creating a potential barrier, Vj, which prevents further diffusion. Thus, the depletion region under equilibrium conditions is the solution of the Poisson's equation, given the charge density profile, which represents the ionized doping atoms on both sides of the junction and considers the fixed positive charges on the P-side and the negative on the N-side. An important concept related to the depletion region is the so-called junction potential. It is the built-in potential barrier, Vj, created at the junction due to the diffusion of charge carriers. The junction potential can be measured relative to the quasi-neutral regions. Vj is strictly linked to the doping concentrations,

Na and Nd, and the physical properties of the semiconductors, for instance, the permittivity ε. When applying an external voltage, either reverse or forward, the total potential profile is modified, resulting in a new depletion width W and junction potential Vj.

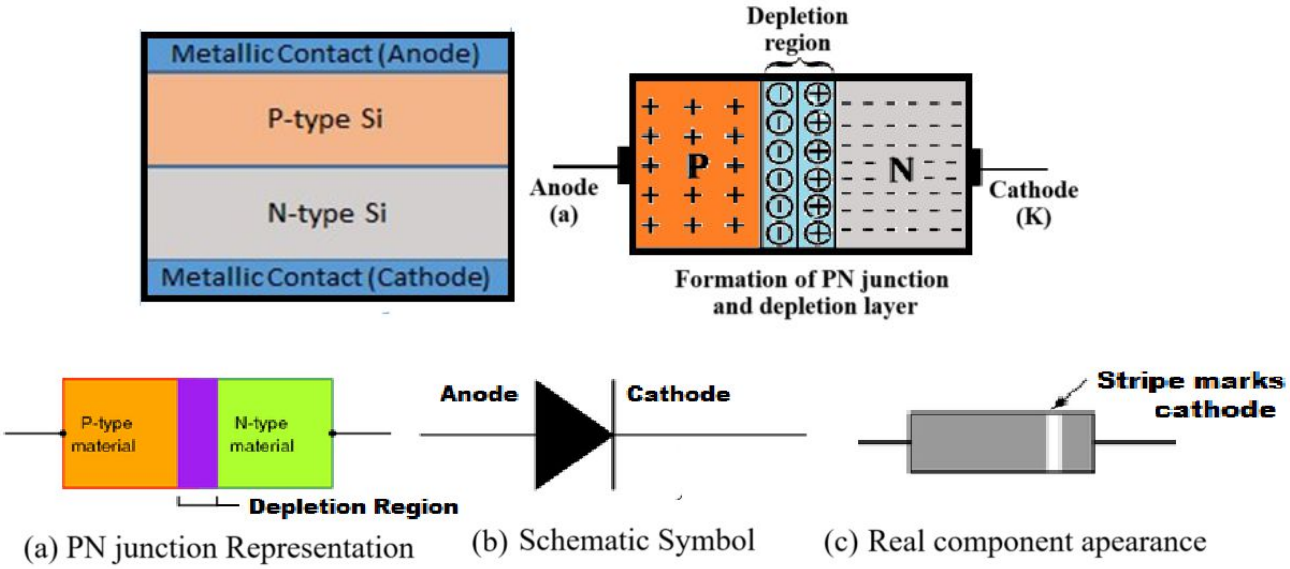

Figure 1 PN junction configurations.

The PN junction can be described by analyzing the carrier recombination and generation processes. Under equilibrium conditions, the rates of recombination and generation are equal. Therefore, the minority carrier concentration is defined by the majority carrier concentration (holes in the N-side) and the band gap energy E_g, where n_i is the intrinsic charge carrier concentration and T is the temperature in Kelvin. On the other side, when a PN junction diode is forward-biased, a voltage is applied that reduces the internal potential barrier. This allows the majority carriers from the P-side (holes) to flow into the N-side, whereas the current will recombine with minority carriers (electrons), thus modifying the concentration profile of charge carriers. The generated current is proportional to the recombination rate and thus the exponential function of voltage V. Conversely, a reverse voltage $V > 0$ applied to the diode widens the depletion region and increases the potential barrier, thus suppressing conduction. As a result, the concentration of minority carriers in the neutral P-side region decreases, leading to a delay in the current generation. This phenomenon is called storage time τs. In this theoretical framework, the description of energy band theory is also relevant to understanding semiconductor behavior. The energy band diagrams describe the discrete energy levels of electrons and holes within the semiconductor materials. At absolute zero temperature, semiconductors behave like insulators since no electrons are thermally excited to conduction bands. The charge carrier concentration is thus a function of thermal energy and energy gap, specifying the conductivity of the semiconductors.

3. Basic Principles

When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called pn junction (Figure 2). At the instant of pn junction formation, the free electrons near the junction in the n region begin to diffuse across the junction into the p region where they combine with holes near the junction. The result is that n region loses free electrons as they diffuse into the junction. This creates a layer of positive charges (pentavalent ions) near the junction. As the electrons move across the junction, the p region loses holes as the electrons and holes combine. The result is that there is a layer of negative charges (trivalent ions) near the junction. These two layers of positive and negative charges form the depletion region (or depletion layer). The term depletion is due to the fact that near the junction, The region is depleted of charge carries (free electrons and holes) due to diffusion across the junction. It may be noted that depletion layer is formed very quickly and is very thin compared to the n region and the p region.

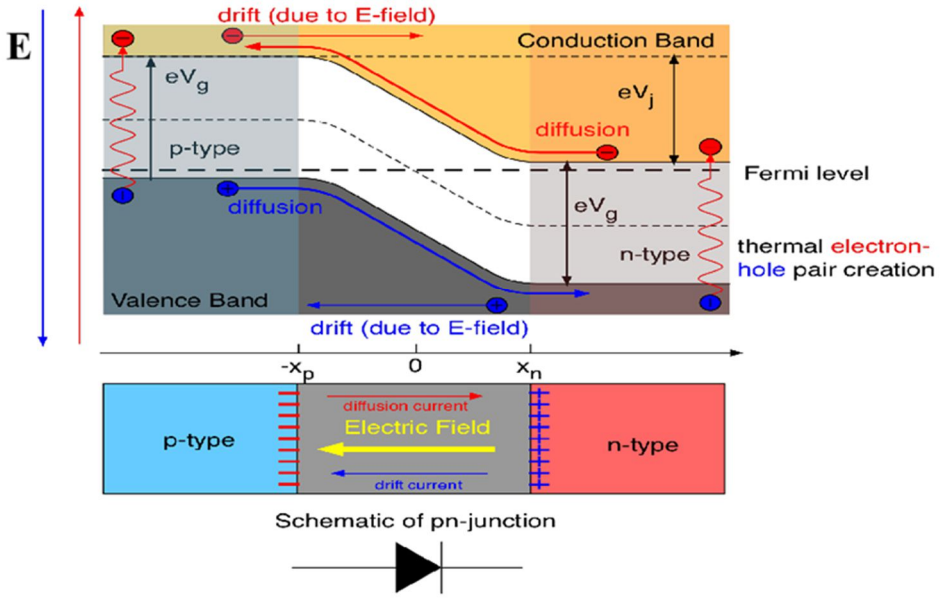

Figure 2 Energy band diagram for a pn junction.

The PN junction can be described by analyzing the carrier recombination and generation processes. Under equilibrium conditions, the rates of recombination and generation are equal. Therefore, the minority carrier concentration is defined by the majority carrier concentration (holes in the N-side) and the band gap energy E_g, where n_i is the intrinsic charge carrier concentration and T is the temperature in Kelvin. On the other side, when a PN junction diode is forward-biased, a voltage is applied that reduces the internal potential barrier. This allows the majority carriers from the P-side (holes) to flow into the N-side, whereas the current will recombine with minority carriers (electrons), thus modifying the concentration profile of charge carriers. The generated current is proportional to the recombination rate and thus the exponential function of voltage V.

Conversely, a reverse voltage V > 0 applied to the diode widens the depletion region and increases the potential barrier, thus suppressing conduction. As a result, the concentration of minority carriers in the neutral P-side region decreases, leading to a delay in the current generation. This phenomenon is called storage time τ_s. In this theoretical framework, the description of energy band theory is also relevant to understanding semiconductor behavior. The energy band diagrams describe the discrete energy levels of electrons and holes within the semiconductor materials. At absolute zero temperature, semiconductors behave like insulators since no electrons are thermally excited to conduction bands.

4. Mathematical Formulation

The P-N junction supports unidirectional current flow. If ($+V_e$) terminal of the input supply is connected to anode (P-side) and ($-V_e$) terminal of the input supply is connected the cathode. Then diode is said to be forward biased as shown in Figure 3(a). In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current from inside (injected minority current due to holes crossing the junction and entering P side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short- circuited switch.

If ($-V_e$) terminal of the input supply is connected to anode (p-side) and ($+V_e$) terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased as shown in Figure 3(b). The Fermi levels in the forbidden gap of the separated semiconductors have different positions. The edge of both the conduction and valence bands of the n type semiconductors will bend up (Figure 3(c)), and both the conduction and valence bands of the p type semiconductors will bend down (Figure 3(c)). The conduction bands of both types will coincide and the valence bands will coincide too. Thermal equilibrium in a pn junction: No temperature gradient throughout sample. Excitation of carriers is unavailable, no current might flow in the pn junction and the net current is equal to zero.

In the p-type region the concentration of holes that are majority is much higher than that of electrons, which are minority carriers. Where:

$$p_o = \frac{n_i^2}{N_D}$$

In the n-type region the concentration of electrons is much larger than that of holes so:

$$n_o = \frac{n_i^2}{N_A}$$

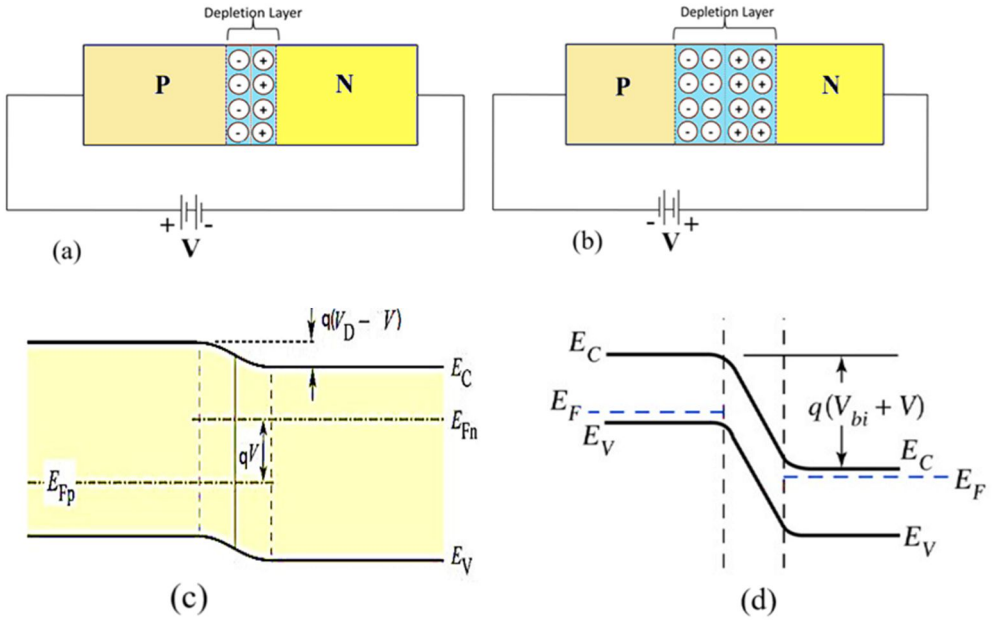

Figure 4 PN (a) Diode in Forward Bias, (b) Reverse Bias, Band structure of a PN junction in (c) forward bias and (d) reverse bias.

In the forward bias, the difference between the Fermi levels of the junction can be expressed by:

$$qV_b = Ef_n - Ef_p$$

In Shockley model of PN junction: The junction is assumed an abrupt, whereas the region out of the space charge region is neutral. The carrier densities at the boundaries are related to the potential distribution. The injected minority carrier density is small in comparison to the majority carrier density.

The depletion region is free of charge, and so generation or recombination cannot occur. The current density passing through an ideal pn junction diode due to applying a voltage (V) is described by the Shockley equation:

$$I = qAn_i^2.\left(\frac{D_h}{L_h N_D} + \frac{D_e}{L_e N_A}\right)\left[\exp\left(\frac{V}{V_T}\right) - 1\right]$$

Where ; q is electron charge, A diode area, D diffusion coefficient, L is diffusion length, V_T thermal voltage, the subscripts p and n refer to holes and electrons.

$$V_T = \frac{K_B T}{q}$$

At room temperature, V_T = 26 mV. The current is:

$$I = I_s\left[exp\left(\frac{V}{V_T}\right) - 1\right]$$

The current I_S is called the saturation:

$$I_s = qAn_i^2.\left(\frac{D_h}{L_h N_D} + \frac{D_e}{L_e N_A}\right)$$

5. Experimental Setup and Procedure

Experiments have been designed to carry out practical work on PN junction diodes, investigating their operational characteristics and applications. Each experiment is self-contained, with background theory and a description of the apparatus required. Consideration is given to the significance of the experimental results, linking them to the theoretical concepts discussed in the previous sections. Each experiment reinforces a particular theoretical aspect by linking it to actual performance. Where necessary, suggestions are made for extending the experiments.

The current-voltage (I-V) characteristics of a diode describe how the current flowing through it changes as a function of voltage across it. These characteristics are typically well understood for a simple ideal diode. However, many real world diodes exhibit behavior not predicted by the ideal diode model. The I-V characteristics of a diode under forward and reverse bias are explored in detail here. In forward bias, the diode is said to be conducting. It is connected in the circuit in such a way that it allows current to flow through it. As a result, a forward biased diode exhibits a relatively low resistance. Under reverse bias, on the other hand, the diode is said to be non-conducting. It is connected in the circuit in such a way that it restricts the flow of current. As a result, a reverse biased diode behaves like an insulator, allowing only a small leakage current. A diode's bias voltage and the current flowing through it can be manipulated by connecting it to different circuit arrangements. In all cases, the diode voltage and current can be expected to be related by a simple mathematical expression.

Step 1:

A plot of a current passing through a diode against an applied voltage is referred to as current – voltage characteristics of the diode. Three different regions are seen:

- At point A: the forward current is zero at zero-bias condition.
- At point B: The current increases slightly until reaches approximately 0.7 V at the knee of the curve.
- After point B, the change in the forward voltage becomes not noticeable.
- At point C: the forward current increases rapidly.

Step 2:

The forward voltage at the point C is approximately equal to the built-in voltage.

- At zero-bias condition, the reverse current is strongly diminished.
- If the reverse-bias voltage is increased, a very small reverse current is seen.
- The reverse current increases rapidly, when only the applied voltage accedes a certain value called breakdown voltage (V_R).

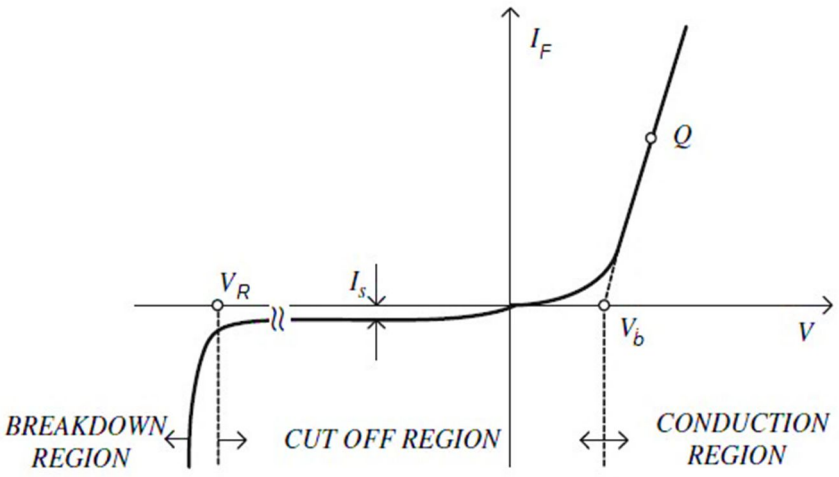

***Figure 5 Characteristics of an ideal pn junction diode*.**

6. Interpreting Results

In experiments involving pn junction, it is conventional to plot relevant results on a graph, with one variable plotted against another. Study material notes on IV characteristics in forward bias and reverse bias, we can get at a fact pn junction diode conducts current only in one direction. during forward bias. During forward bias, the diode conducts current with an increase in voltage. During reverse bias, the diode does not conduct with an increase in voltage.

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PN Junction Practical Section

1. Instrumentation

The PN junction diode, Regulated Power Supply, Resistors, Ammeter, Voltmeter, Bread Board, Connecting wires.

2. Principle and Working

A diode is a nonlinear circuit element. Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n junction diode with a junction called depletion region (this region is depleted off the charge carriers) as shown in Figure 1. This region gives rise to a potential barrier called Cut-in Voltage. This is the voltage across the diode at which it starts conducting. The pn junction can conduct beyond this potential.

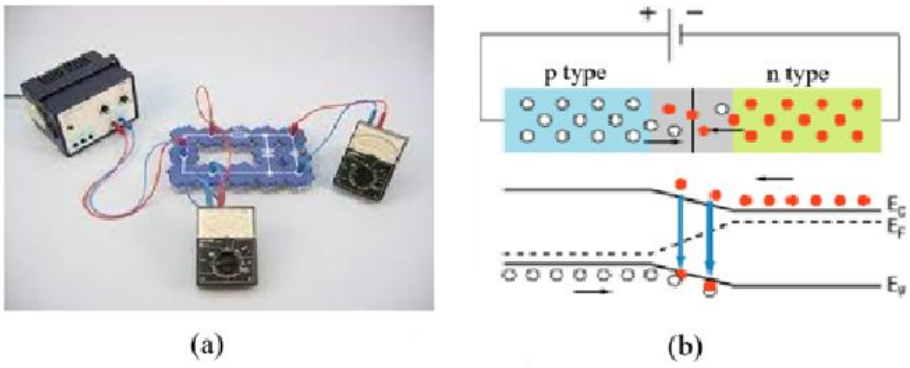


Figure 1 (a) Instrumentation and (b) operating principle.

3. Target of the experiment

To draw IV characteristic of pn junction diode and to determine knee or cut in voltage and calculate dynamic resistance and cut-in voltage from graph for the given diode (Figure 2).

The voltage current equation for diode is given by following formula:

$$I = I_0 (e^{V/\eta VT} - 1)$$

Here, I is current through diode and V is Applied voltage to the diode. V_T is voltage equivalent to temperature (KT/q) and η is constant (η =1 for Germanium and η = 2 for Silicon).

- **In forward bias**

When $V_F = +V$, then $e^{V/\eta VT} > 1$, thus :

$$I_F = I_0\, e^{V/\eta VT}$$

Hence, the theoretical analysis indicates that forward current increases exponentially with voltage. But, practically it is not found because pn junction diode has a certain barrier /threshold/knee potential. Initially the applied forward potential to diode is used to neutralize this barrier potential (Figure é(b)).

- **In reverse bias**

When $V_R = -V$, then $e^{V/\eta VT} < 1$, thus:

$$I_R = -I_0$$

Thus in reverse bias of diode (Figure 2(b)), a constant current flows through the diode whose direction is opposite to forward bias current. This current is known as reverse saturation current and it is independent of voltage. At large reverse bias voltage, the reverse bias current increases gradually to maximum due to avalanche breakdown.

4. Experimental Procedure

1. Connections are made as per the circuit diagram.
2. For forward bias, the ($+V_e$) supply is connected to the anode of the diode and ($-V_e$) supply is connected to the cathode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage (V_F) on X-axis and current (I_F) on Y-axis.

5. Results and discussion

- **Forward bias**

The non-destructive usage characteristics of diodes are: I_{max} =1 A, P_{max} = 1.1 W and $U_{R(inv)max}$ = 1000 V. Circuit of Figure 1 realized. Adjust the power supply to have a voltage drop V_F = 0.1 V across the terminals of diode D. The current intensity I_F passing through diode D is 0 mA. The value of the forward resistance of diode D is:

$$R_F = U/I = 0.1/0 = \text{infinite.}$$

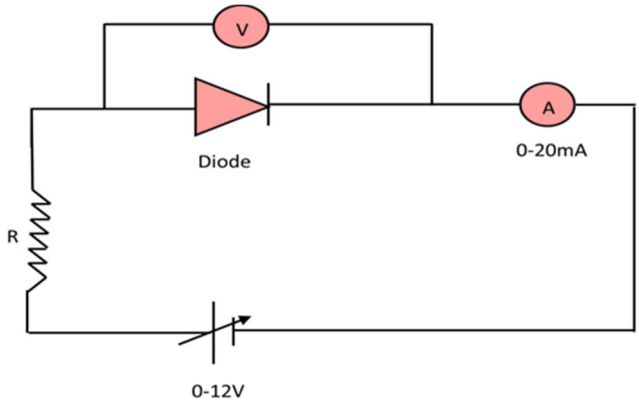


Figure 2 Forward Biasing of PN Junction Diode.

Table 1 for forward bias voltage and forward current is presented below:

V_F(V)	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.75
I_F(mA)	0	0.000	0.000	0.000	0.009	0.120	1.120	10.800	30.200

Curve made with Table 1 is illustrated in Figure 3.

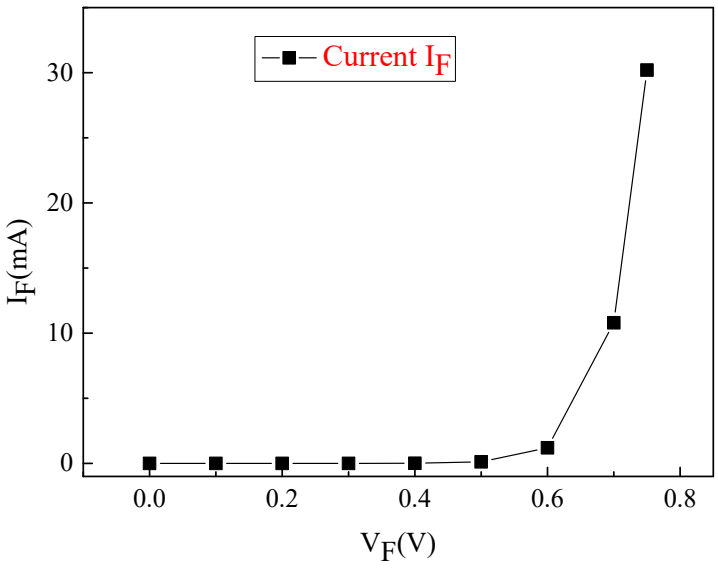


Figure 3 Variation of forward bias voltage and forward current.

Analyzing this curve, we realize that whatever the voltage, a current flows through the diode. In this state, the diode conducts the current and has a low resistance.. The dynamic resistance for forward bias is:

$$R_F = \Delta V_F / \Delta I_F = 0.15/0.02 = 7.5\ \Omega$$

➢ **In reverse bias**

Circuit of Figure 4 realized. Adjust the power supply to have a voltage drop $V_R = -2V$ across the terminals of diode D. The intensity of the current I_R passing through diode D is 0.2 µA. The value of the forward resistance of diode D is:

$$R_R = U/I = -2/0.0000002 = 10\ M\Omega$$

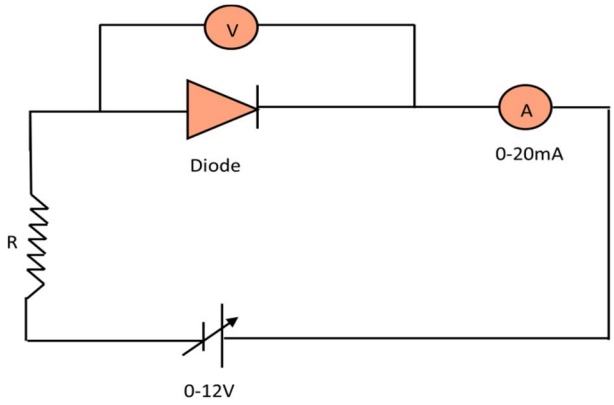


Figure 4 Reverse Biasing of PN Junction Diode.

Table 2 for reserve bias voltage V_R and reserve current I_R is presented below:

V_R (V)	**0**	**-2**	**-5**	**-7**	**-10**	**-11**	**-12**	**-13**	**-14**	**-15**	**-18**	**-20**
I_R(µA)	0.0	0.2	0.5	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.8	2.0

Curve made with Table 2 is illustrated in Figure 5.

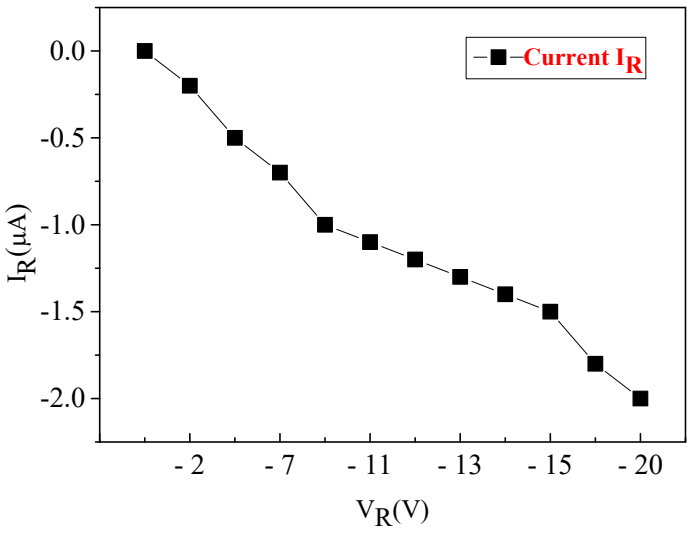
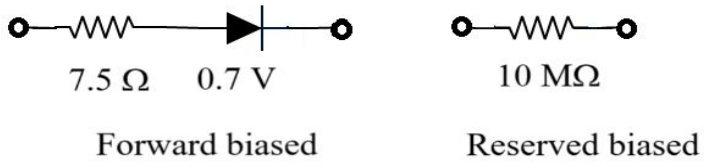


Figure 5 Variation of for reserve bias voltage and reserve current.

By analyzing this curve, we realize that whatever the voltage, a negligible current flows through the diode. The diode blocks the current like an open switch. The dynamic resistance for reserve bias is:

$$R_R = \Delta V_R / \Delta I_R = 20/0.000002 = 10\ M\Omega$$

Equivalent models in forwarded biased and reserved biased are:



✓ **Error analysis**

Instrumental error

For constant magnetic field, the percentage error in calculating hall co-efficient,

$$\frac{dR}{R} = \left(\frac{dI}{I} + \frac{dV}{V}\right) \times 100$$

Where, dI = least count in probe current measurement = 0.01 mA and dV = least count in hall voltage measurement = 0.1 volt

$$\frac{dR}{R}\% = \left(\frac{dI}{I} + \frac{dV}{V}\right) \times 100 = 1.9\%$$

Questions / Discussions:

1) What happens when the battery voltage is increased in a forward-biased P-N junction?

The current through the junction increases when the battery voltage is increased in a forward-biased P-N junction.

2) What happens when a P-N junction is reverse biased?

The holes and electrons tend to move away from the junction.

3) What is the static resistance of a diode?

Static resistance of a diode is defined as the ratio of the DC voltage applied across the diode to the DC current flowing through the diode.

4) What is the dynamic resistance of a diode?

Dynamic resistance of a diode is defined as the ratio of change in voltage to the change in current.

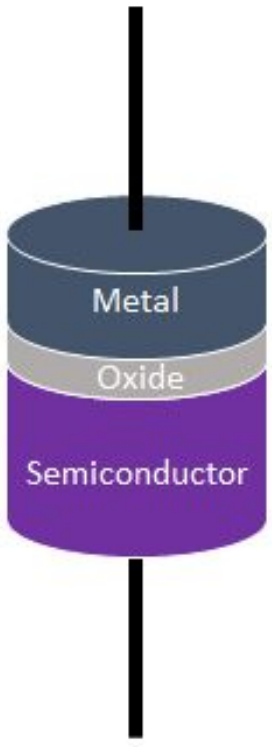
5) What is reverse resistance?

Reverse resistance is defined as the resistance offered by the P-N junction diode when it is reverse biased.

Practical Works 03

MOS Capacitors

L3 physics of materials



By Dr. GACEM Amel

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1. Introduction

Metal-Oxide-Semiconductor (MOS) capacitors are integral parts of almost every semiconductor device, whether they are discrete or part of an integrated circuit. They are the simplest and earliest devices envisioned using the MOS structure, and their understanding is crucial to comprehending more complex devices built upon the same principles. At the most basic level, a capacitor is a two-terminal device that stores charge. MOS capacitors consist of a metal gate electrode, an insulating layer of oxide, and a semiconductor. It is essential to understand the basic principles of operation of MOS capacitors since they are the building blocks of metal-oxide-semiconductor field-effect transistors (MOSFETs), the most widely used transistors in modern electronic applications. Almost every technology built around the MOSFET relies on the accurate, repeatable formation of MOS capacitors. MOS capacitors are simplest from a processing point of view. After growing an oxide layer on a clean semiconductor surface, the device is completed by depositing a metal electrode to form an MOS capacitor.

Since most of the present-day transistors are built using the MOSFET technology, it is essential to understand the principles of operation of the MOS capacitors on which the MOSFET is based. Moreover, the power of one technology that guarantees low-cost, high-performance devices compliant with ever-shrinking geometries hinges upon detailed comprehensive academic investigations of the individual components of the technology. MOS capacitors are used mostly for process control monitoring, the reliability assessment of the oxide, and measurement of the fixed charge present at the oxide-silicon interface. MOS capacitors are perhaps the most widely used fundamental three-terminal devices in the IC technology and probably the simplest ones to fabricate since they need just the oxide growth followed by the metal deposition steps. However, it is the miscomprehension of the basic principles of this simple device that led to questions and doubts regarding the validity of experiments and the interpretation of results involving more complex devices. Modern devices are paroxysms of elaboration and complexity involving the interaction of several physical mechanisms. MOS capacitors, on the other hand, are the simplest devices conceivable having well-understood electrostatic and other characteristics.

2. Definition

A Metal-Oxide-Semiconductor (MOS) capacitor is a fundamental structure used extensively in semiconductor device technology, particularly in the fabrication of integrated circuits and MOSFETs (metal-oxide-semiconductor field-effect transistors). The MOS capacitor consists of three layers: a metal gate, a dielectric oxide, and a semiconductor substrate. The metal gate is typically made from highly conductive materials such as aluminum or polysilicon. Beneath the metal gate lies a thin layer of insulating oxide, usually silicon dioxide (SiO2), which is the dielectric. The semiconductor substrate is commonly silicon, which can be either p-type or n-type (Figure 1).

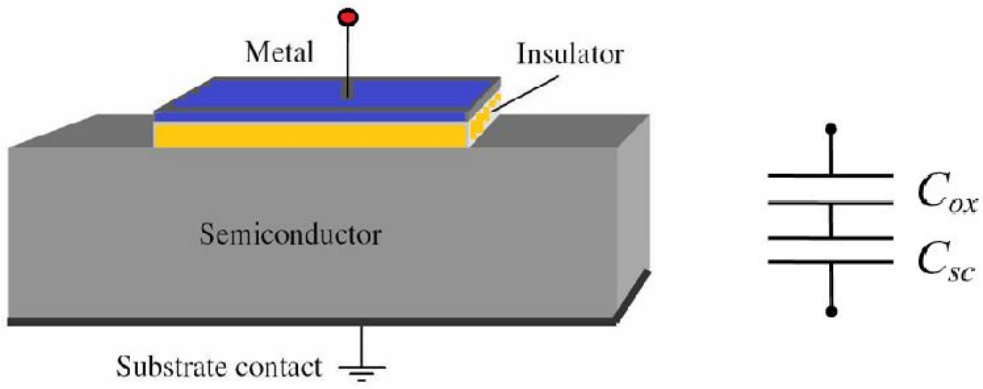

Figure 1 MOS capacitor configuration.

3. Functional Basic Principles

When a voltage is applied to the metal gate, it influences the distribution of electrical carriers in the semiconductor. The semiconductor's energy bands are flat at zero applied voltage, indicating no excess charge within the oxide or at the semiconductor surface. As the gate voltage is increased positively, it attracts electrons towards the interface of the oxide and the semiconductor. This creates an accumulation of electrons in n-type silicon and a depletion of holes in p-type silicon, forming the depletion layer. A further increase in the voltage leads to strong inversion, where the semiconductor surface beneath the oxide changes its type; for example, a p-type becomes an n-type, as electrons become the majority carriers. This inversion layer is critical in the operation of MOSFETs. The capacitance of the MOS structure varies with the voltage applied to the gate.

The capacitance-voltage method C(V) is the most widely used electrical characterization method to evaluate the amount of charges in the insulator of a MOS structure. The measurement of

the capacitance of the structure is carried out with an impedance meter by applying an alternating voltage of a few millivolts superimposed on a direct voltage. The capacitance of the MOS structure varies with the applied direct component Vg: thus, the structure is studied for the different operating regimes (cf.0). The equivalent electrical diagram of a perfect MOS structure (without interface states) is shown in Figure 2. The MOS structure is modelled by the series association of two capacitances: the capacitance of the oxide Cox and that of the semiconductor C_{sc} (Figure 3(a)). The contribution of the interface states slightly complicates this diagram, with the parallel connection of C_{sc}, of a capacitance C_{ss} in series with a resistor R_{ss} (Figure 3(b)). This method is especially interesting when the contribution of the charge trapped in the oxide remains preponderant compared to that of the interface.

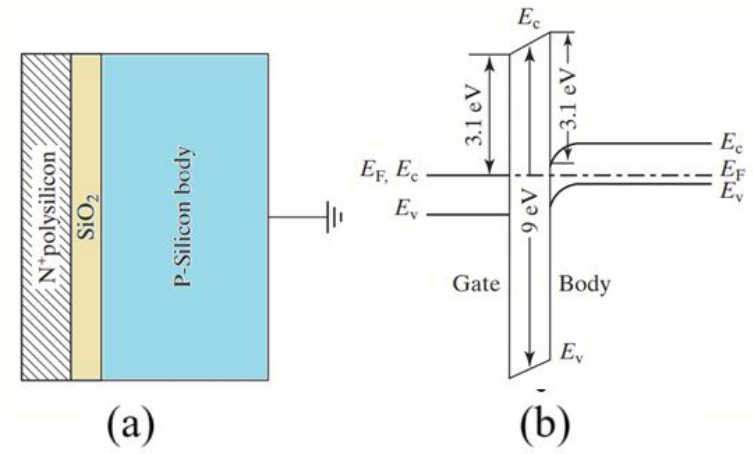

Figure 2 (a) MOS capacitor and (b) Energy band diagram.

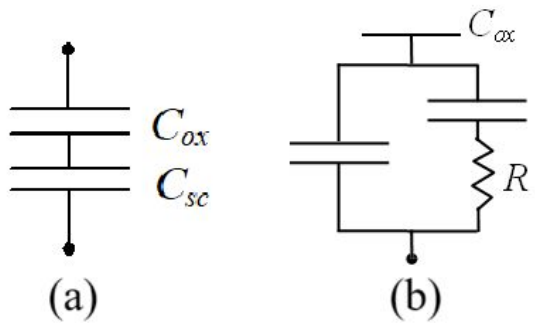

Figure 3 Equivalent diagram of a MOS structure.

4. Mathematical Formulation

The Metal-Oxide-Semiconductor (MOS) structure is a very common structure in microelectronics and power electronics because it is a fundamental part of the transistor. The equivalent electrical capacitance of the structure corresponds to the capacitance of the oxide C_{ox} in series with the capacitance created at the insulator-semiconductor interface C_{sc}. It is written as:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}}$$

As in a capacitor, the charge accumulated in the substrate is equal to the charge accumulated on the grid:

$$Q_m = -Q_{sc} = \frac{\varepsilon_{ox}}{d} V_g \left[C.m^{-2} \right]$$

With ε_{ox} the dielectric permittivity of the oxide and d the thickness of the oxide. Since the carriers are accumulated at the insulator-semiconductor interface, in a first approximation, the capacitance of the interface can be negligible and the equivalent capacitance of the structure is then written:

$$\frac{1}{C} = \frac{1}{C_{ox}}$$

The evolution of the capacitance value of the P substrate and N substrate MOS structure as a function of the gate potential Vg is shown at high and low frequency in Figure 4.

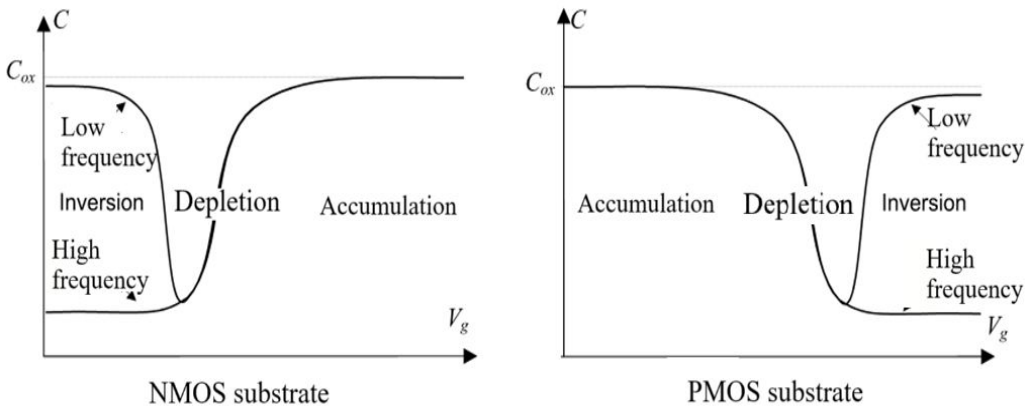

Figure 4 C(V) curves of a MOS capacitor for two types of substrate.

The C(V) measurement allows the thickness of the oxide d to be determined by the relation:

$$C_{ox} = \frac{\varepsilon_{ox} S}{d}$$

With C_{ox} the capacity of the structure in accumulation mode measured in Farad, S the surface of the electrode of the capacity, ε_{ox} the dielectric permittivity of the oxide and d the thickness of the oxide. The three operating regimes of MOS structures are clearly visible on the C(V) curves :Inversion, depletion and accumulation. The C(V) characteristic of the real MOS structure can exhibit various deviations from the ideal curve. These deviations are linked, among other things, to defects present in the insulator or at the interface.

5. Experimental Setup and Procedure

CV characterization of MOS capacitors using the 4200A-SCS. This test performs a capacitance measurement at each step of a user-configured linear voltage sweep. A CV graph is generated from the acquired data, and several device parameters are calculated using the Formulator, which is a tool in the 4200A-SCS's software that provides a variety of computational functions, common mathematical operators, and common constants.

6. Data Analysis and Interpretation

This section describes how the data obtained from the experiments are processed and interpreted to extract useful results.

7. Interpreting Results

In experiments involving the MOS transistor, it is conventional to plot relevant results on a graph, with one variable plotted against another. Here is explored how key results are affected by several important factors. These are important in order to contextualize what was found in the experiments. Results that are considered beyond the central four experiments may also be of relevance in understanding the effect of material properties on MOS transistor.

References

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MOS Capacitors Practical Section

1. Target of the experiment

The objective of this laboratory activity is to determine the most important characteristic of MOS capacitor is that its capacitance changes with an applied DC voltage. Therefore, the operating modes of MOS capacitor change depending on the applied voltage. Since, when a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion and inversion regions.

2. Procedure

Performing C-V measurements with the 4210-SCS simulator to simplify the tests We were able to perform CV measurements on a MOS capacitor and its parameters (Figure 1). Knowing that, the 4200A-SCS is a modular, customizable, and fully-integrated parameter analyzer that provides synchronized insight into current-voltage (IV), capacitance-voltage (CV), and ultra-fast pulsed IV electrical characterization. Its optional 4200A-CVIV Multi-switch Module enables effortless switching between IV and CV measurements without re-cabling or lifting prober needles. The highest performance analyzer, the 4200A-SCS accelerates testing of complex devices for materials research, semiconductor device design, process development, or production.

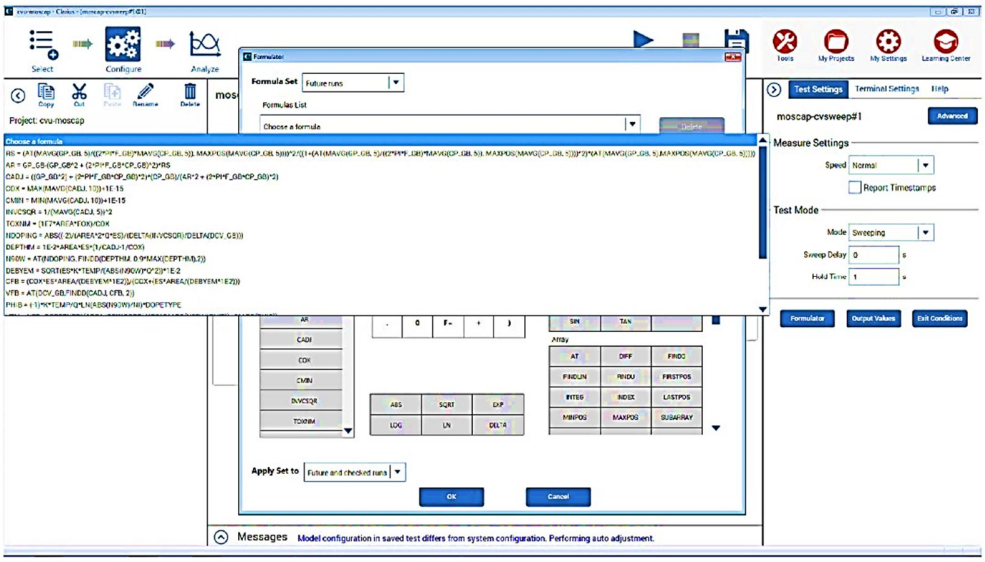


***Figure 1** Simulator window with parameters derived.*

<u>Step 1 :</u> Variation of CV MOS capacitor

The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. Figure 2 illustrates a high frequency CV curve for a p type semiconductor substrate. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

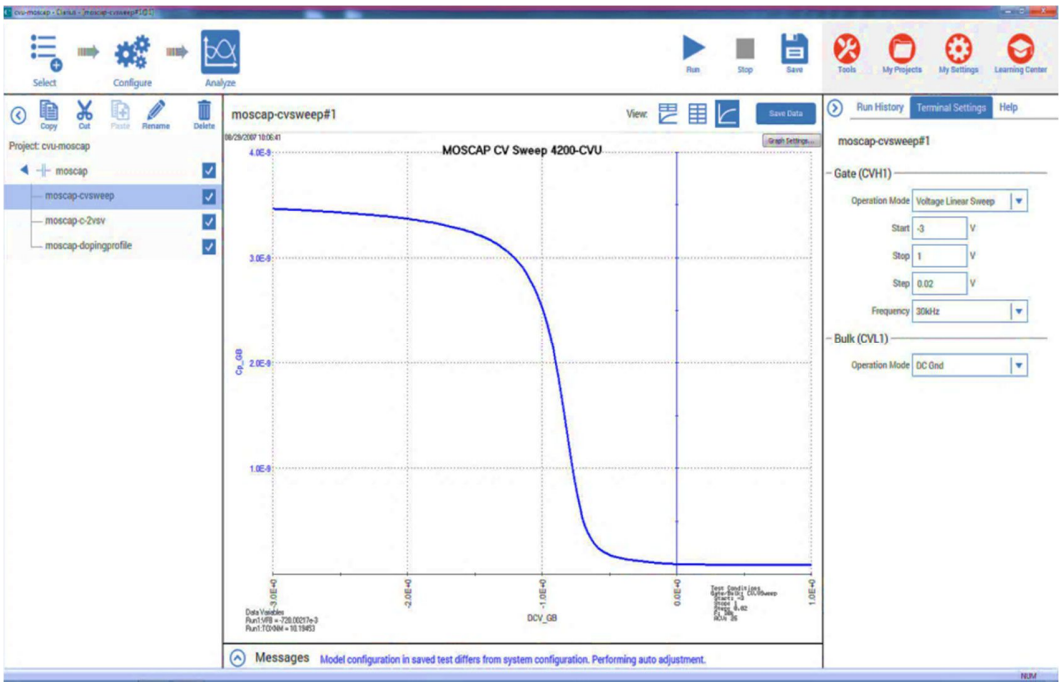


Figure 2 CV curve of a p type MOS capacitor measured.

We notice the appearance of three modes of operation, accumulation, depletion and inversion for the case of a p-type semiconductor (Figure 3). For a p-type MOS, as the gate voltage increases beyond the threshold voltage, dynamic carrier generation and recombination2 move toward net carrier generation. The positive gate voltage both generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrateto-oxide/ well-to-oxide interface. The accumulated minority carrier layer is called the inversion layer, because the carrier polarity is inverted. Above a certain positive gate

voltage, most available minority carriers are in the inversion layer, and further gate voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth.

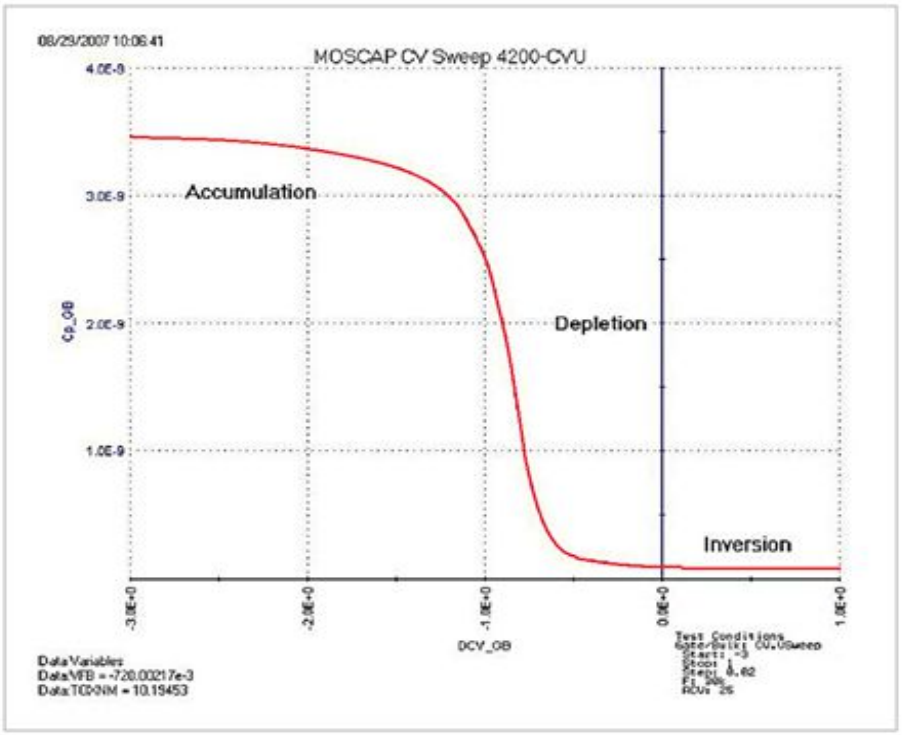


Figure 3 Modes of operation for a p type MOS.

<u>Step 2:</u> Variation of I/C^2 with Gate Voltage

Figure 4 shows the window of the Formulator. These derived parameters are listed in the analyse view of the test.

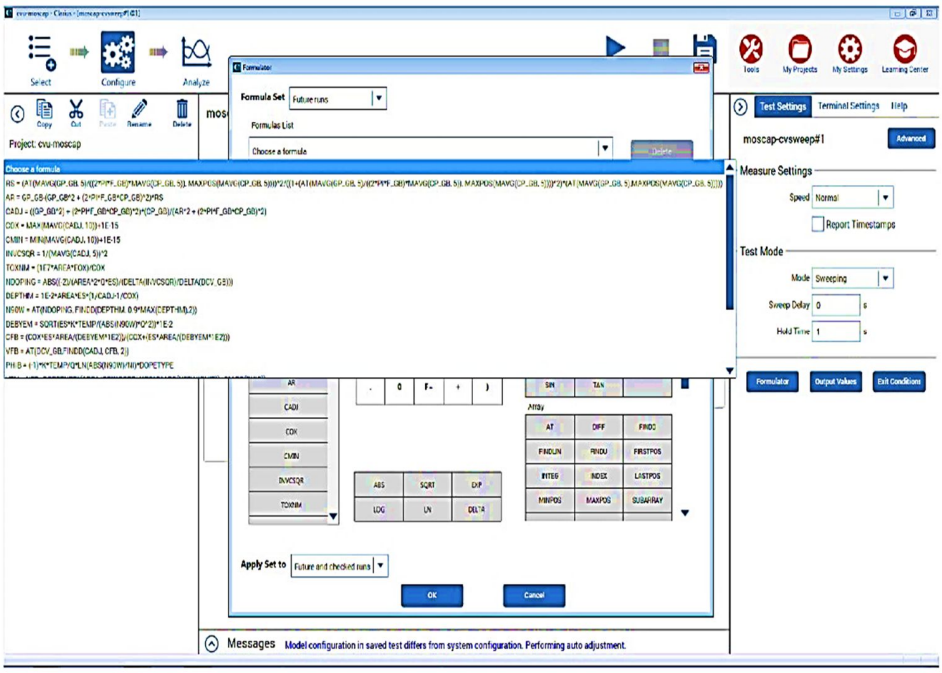


Figure 4 Simulator with parameters derived.

The variation of capacitance ($1/C^2$) as a function of the gate voltage (V_G) is presented in Figure 5.

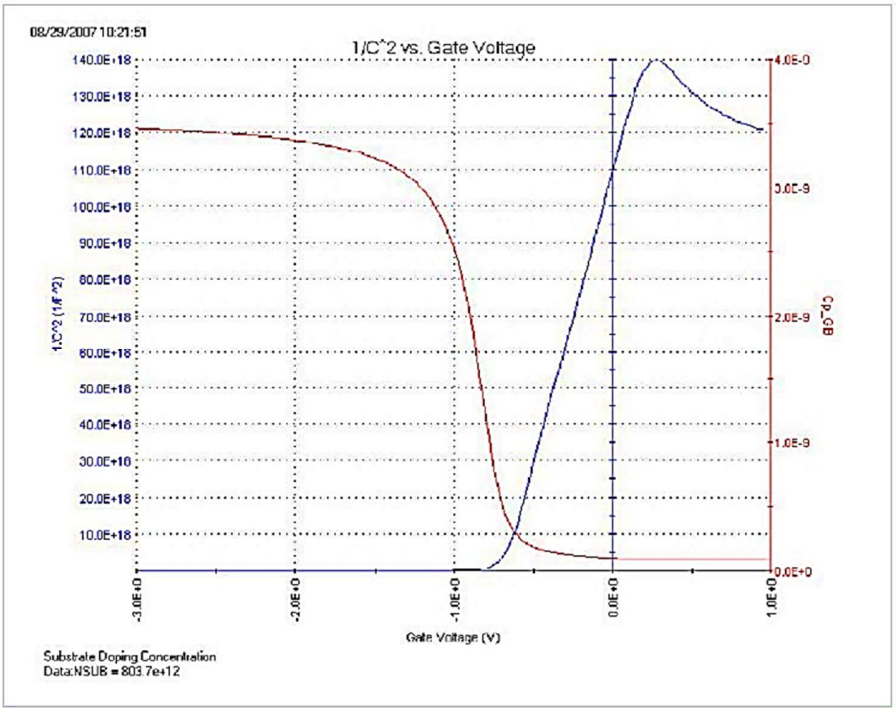


Figure 5 Variation of $1/C^2$ via gate voltage.

3. Analysis of results

Step 1 :

As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions (Figure 3).

- **Inversion Region**

As the gate voltage of a p-type MOS-C increases beyond the threshold voltage, dynamic carrier generation and recombination move toward net carrier generation. The positive gate voltage generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide/well-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate voltage increases do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth. Once the depletion region reaches a maximum depth, the capacitance that is measured by the high frequency capacitance meter is the oxide capacitance in series with the maximum depletion capacitance. This capacitance is often referred to as minimum capacitance. The C-V curve slope is almost flat. The three modes of operation, accumulation, depletion and inversion, will now be discussed for the case of a p-type semiconductor, then briefly discussed for an n-type semiconductor at the end of this section.

- **Accumulation Region**

With no voltage applied, a p-type semiconductor has holes, or majority carriers, in the valence band. When a negative voltage is applied between the metal gate and the semiconductor, more holes will appear in the valence band at the oxide-semiconductor interface. This is because the negative charge of the metal causes an equal net positive charge to accumulate at the interface between the semiconductor and the oxide. This state of the p-type semiconductor is called accumulation. For a p-type MOS capacitor, the oxide capacitance is measured in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the C-V curve is almost flat. This is where the oxide thickness can also be extracted from the oxide capacitance. However, for a very thin oxide, the slope of the C-V curve doesn't flatten in accumulation and the measured oxide capacitance differs from the actual oxide capacitance.

- **Depletion Region**

When a positive voltage is applied between the gate and the semiconductor, the majority carriers are replaced from the semiconductor-oxide interface. This state of the semiconductor is called depletion because the surface of the semiconductor is depleted of majority carriers. This area of the semiconductor acts as a dielectric because it can no longer contain or conduct charge. In effect, it becomes an insulator. The total measured capacitance now becomes the oxide capacitance and the depletion layer capacitance in series, and as a result, the measured capacitance decreases. This decrease in capacitance is illustrated in Figure 3 in the depletion region. As a gate voltage increases, the depletion region moves away from the gate, increasing the effective thickness of the dielectric between the gate and the substrate, thereby reducing the capacitance

Step 2:

This test performs a CV sweep and displays the capacitance $1/C^2$ as a function of the gate voltage V_G (Figure 4). A positive slope indicates acceptors and a negative slope indicates donors. The substrate doping concentration is extracted from the slope of the $1/C^2$ curve and is displayed on the graph.

For a relatively thick oxide (> 500Å), extracting the oxide thickness is fairly simple. The oxide capacitance (C_{ox}) is the high-frequency capacitance when the device is biased for strong accumulation. In the strong accumulation region, the MOS capacitor (MOS-C) acts like a parallel plate capacitor and the oxide thickness may be calculated from C_{ox} and the gate area using the following equation:

$$T_{ox} = A\ (\varepsilon_{ox} / C_{ox})$$

Here A is the gate area of metal = 10^{-2} cm^2, ε_{ox} = 34.515x10^{-14} Fcm^{-1}, C_{ox} is oxide capacitance measured by CV curve for Accumulation region = 65 pF by Fig. 3. So after the calculation value of T_{ox} comes 510 Å. The C-V characteristics of MOS capacitors contain a wealth of information about the semiconductor characteristics, which extend to MOS. When simplify and automate both the sweeping of C-V curves. Through the data acquisition system characteristic curve war obtained with a scanning capacitance in voltage of a MOS capacitor. From the data obtained through the data acquisition system is able to obtain the thickness of the oxide in a MOS capacitor.

Questions / Discussions:

1) An MOS capacitor biased so that majority carriers in the semiconductor pile up at the oxide semiconductor interface is biased in which region?

In accumulation region.

2) The capacitance of an MOS capacitance can be represented as a series combination of two capacitors. What are the two capacitors?

The oxide capacitance and the semiconductor capacitance (accumulation, depletion, or inversion depending on the gate bias).

3) In which region is the temporal response of an MOS capacitor the slowest

In inversion region.

4) The minority carrier charge (in C/cm2) is an important quantity for an MOS capacitor. How does it vary with surface potential and with gate voltage above threshold.

Exponentially with surface potential and linearly with gate voltage.

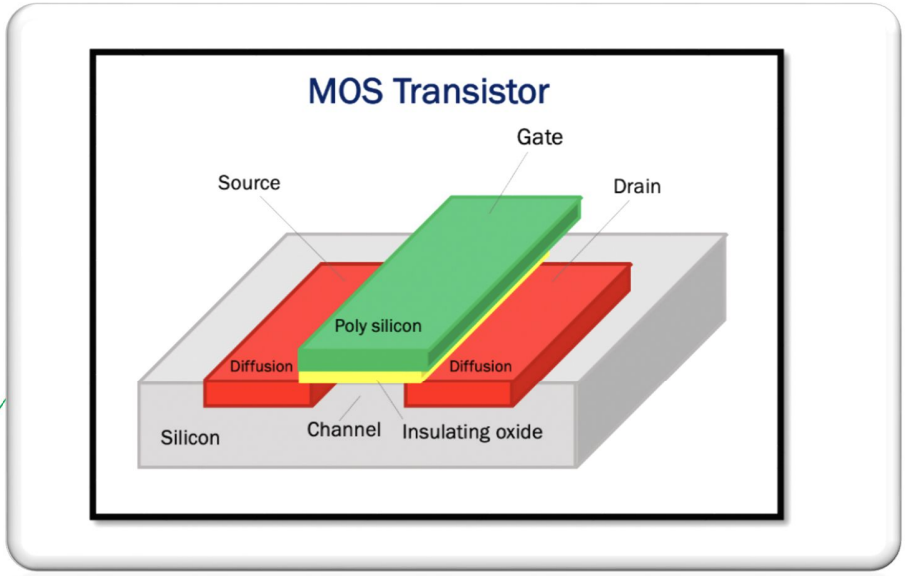
5) The low-frequency MOS capacitance when biased in inversion is a little less than the oxide capacitance, C_{ox}. Why?

Because the inversion layer has a finite thickness.

Practical Works 04

MOS transistors

L3 physics of materials



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MOS Transistors Theatrical Section

1. Introduction

The metal-oxide-semiconductor (MOS) transistor is one of the most prolific devices in the history of electronics, and today, it is difficult to envisage a world without them. From digital watches to smartphones, computers to HD TVs, electric or hybrid vehicles to space satellites, anywhere there is a circuit, there are MOS transistors. It is commonly accepted that the MOS transistor has shaped the way circuits are designed, age-old functionalities are redefined, and new possibilities are explored. Typically, one would say a MOS transistor is made of three terminals: gate (G), drain (D), and source (S) that control the electrical current from drain to source. However, that is not the whole picture. A MOS transistor is built on a wafer that is either made of p type (positively doped with holes) or n type (negatively doped with electrons) semiconductor. For an n-channel MOSFET, the device construction consists of creating two highly doped n-wells (source and drain) inside the p-type substrate. On top of these wells, a layer of metal is deposited on the wafer oxide that creates a gate terminal. Underneath this gate terminal, a thin layer of SiO_2 or high-k materials serves as an insulator between the gate and the channel (p-type substrate). By applying a positive gate voltage, electrons travel from the source well to the drain well through the n-channel formed in the p-type substrate underneath the gate oxide. The opposite occurs in the case of a p-channel MOSFET.

The evolution of the MOS device into a multi-gate shaped architecture has been essential in maintaining Moore's law and logically scaling devices down in size, which means fitting more number of devices into an area unit. Aberrantly, the industry focus is shifting towards beyond-silicon material systems that need to be deeply understood from a basic science point of view.

To this end, a rapid yet practical exploration of n-channel and p-channel MOSFETs with different gate shapes, oxides, and dimensions is presented. In addition, basic electrical characterizations such as transfer, output, and short-circuit current measurements are demonstrated so that essential parameters like threshold voltage, sub-threshold swing, drain-induced barrier lowering, transconductance, and current walk-out can be extracted. Lastly, a short guideline is provided for the reproducibility of these practical experiments.

2. Definition

Metal oxide Semiconductors transistors, often referred to as MOS, come in two types, n channel and p channel (Figure 1(a)). In the basic structure of all MOS transistors, there are two conductive regions called the source and drain, which are connected to an inversion layer conducting channel. This channel is formed by a very thin layer of n or p type semiconductor and is insulated from the conducting gate by a thin layer of silicon oxide (SiO_2). The gate voltage induces carriers (electrons or holes) in the channel, forming an inversion layer, allowing current to flow from the source to drain (Figure 1(b)). This current is controlled by the gate voltage, with the MOS transistor turned on when the gate voltage is above some threshold voltage (V_T). If the gate voltage is set to 0V, the channel is not formed and no current flows from the source to the drain (absolute cut-off). Because of this action, MOS transistors can be used as building blocks for digital logic I_{Cs}.

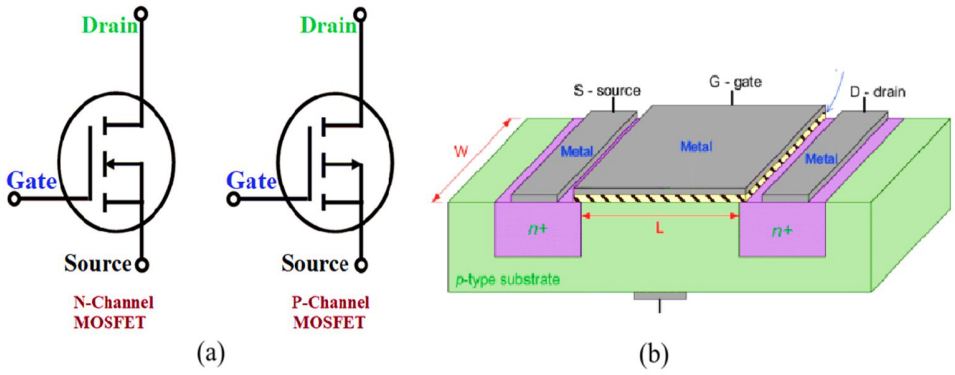

Figure 1 MOS transistor configuration (a) symbol and (b) MOSFET Structure.

3. Basic Principles

The basic operating principles of a MOS device can be explained within the context of an NMOS device as shown in Figure 2. Figure 2(a) shows the device in the "Off" state with the gate, source and drain voltages at zero and the bulk substrate connected to ground. Two pn junctions exist between the n type source/drain regions and the bulk p type substrate. In operation, the potential between the drain and source (V_{DS}), and that between the gate and source (V_{GS}), are always positive. When a small voltage, (V_{GS}) is applied to the gate, the charge carrying holes in the p type substrate are repelled away from the substrate surface. When V_{GS} reaches a threshold value (V_{TH}, the minimum gate to source voltage needed to turn the device on; this is less than the 0.7 V required in BJTs, typically 0.2- 0.25 V in modern logic processors), the region under the gate

becomes completely depleted of charge, producing a region in the substrate called the "depletion zone". Further increases in V_{GS} attract electrons from the electron-rich source (V_{GS}) and drain (V_{GD}) regions into the region under the gate, producing an n+ region known as the "inversion layer", shown in Figure 2(b). This inversion layer is a conducting channel that connects the two n type regions at the source and drain; it will allow electrons to flow from the source to the drain when there is a positive voltage, V_{DS}, between the source and drain. To assure that the induced inversion channel extends all the way from source to drain, the MOS gate structure slightly overlaps the edges of source and drain (the latter is achieved by a method known as a self-aligned process.

When a drain-source bias, V_{DS}, is applied to a NMOS device in the above threshold conducting state, electrons move in the channel inversion layer from source to drain. At relatively small values of V_{DS}, the IV characteristics of the device are linear with ID (drain current) increasing with increasing VD (drain voltage), as shown in Figure 2(b). When the drain voltage is increased to a value known as the saturation voltage, V_{SAT}, the charge and current flow characteristics in an NMOS device evolve, as depicted in Figure 2(c).

The inversion layer under the gate becomes wedge shaped, wider (or deeper) near the source and essentially disappears (zero thickness) at the drain. This phenomenon is known as "pinch-off" and the point where the inversion layer thickness is reduced to zero is called the "pinch-off point". When the voltage applied to the drain is increased beyond V_{SAT}, the pinch off point moves further towards the source, reducing the effective channel length, Leff, as shown in Figure 2(d).

Under these conditions, the area between the pinch-off point and the drain is fully depleted with no inversion layer. Since this region has no positive free carriers, there is no possibility for electron-hole recombination if an electron enters the region from the electron-rich source and, if there is an electric field across the depletion zone, the electron can freely transit to the drain.

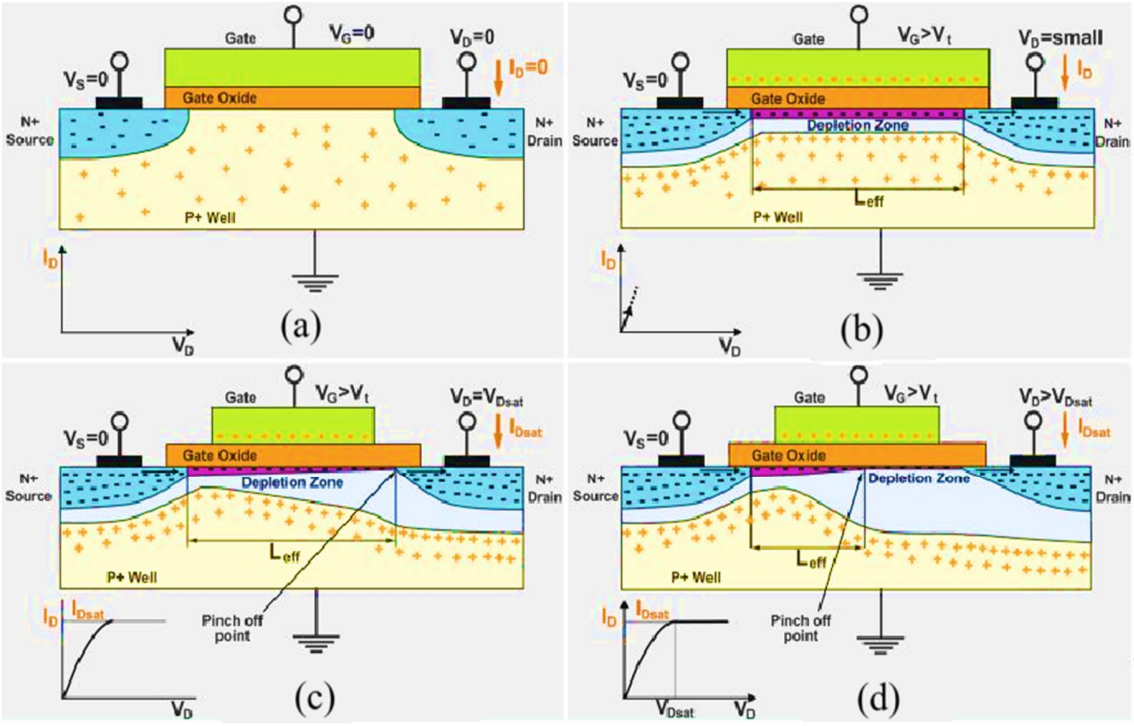

Figure 2 Operating characteristics of NMOS transistor.

4. Mathematical Formulation

For the PMOS transistor, V_{SG} is used and it is usually positive while V_{SD} is always positive (since we have defined the source to be the drain/source terminal with the higher voltage). For both NMOS and PMOS transistors, the gate is insulated from the channel of the transistor resulting in the current going into the gate, $I_G = 0$. Threshold voltage is:

$$V_T = V_{T0} + \gamma(\sqrt{\phi_B + V_{SB}} - \sqrt{\phi_B})$$

- **Saturation region (V_{DS}>V_{GS}-V_T)**

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \mu C_{ox}\frac{W}{L}(V_{GS} - V_T) \approx \frac{2I_D}{V_{GS} - V_T} \approx \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2\lambda \approx \lambda I_D = \frac{\lambda'}{L} I_D$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{\phi_B + V_{SB}}}$$

- **Linear region (V_{DS}<V_{GS}-V_T):**

$$I_D = \mu C_{ox}\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)(1 + \lambda V_{DS})$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \mu C_{ox}\frac{W}{L}V_{DS}$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \approx \mu C_{ox}\frac{W}{L}(V_{GS} - V_T - V_{DS})$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{\phi_B + V_{SB}}}$$

A plot of I_D vs V_{SD} looks the same as the NMOS plot except that the horizontal axis becomes V_{SD} and various V_{SG} values are plotted as shown below (Figure 3). For this example: $V_{tp} = -0.3V$; $\mu_p C_{ox} = 240\mu A/V^2$; $W/L = 100$; $\lambda_p = -0.1mA/V$.

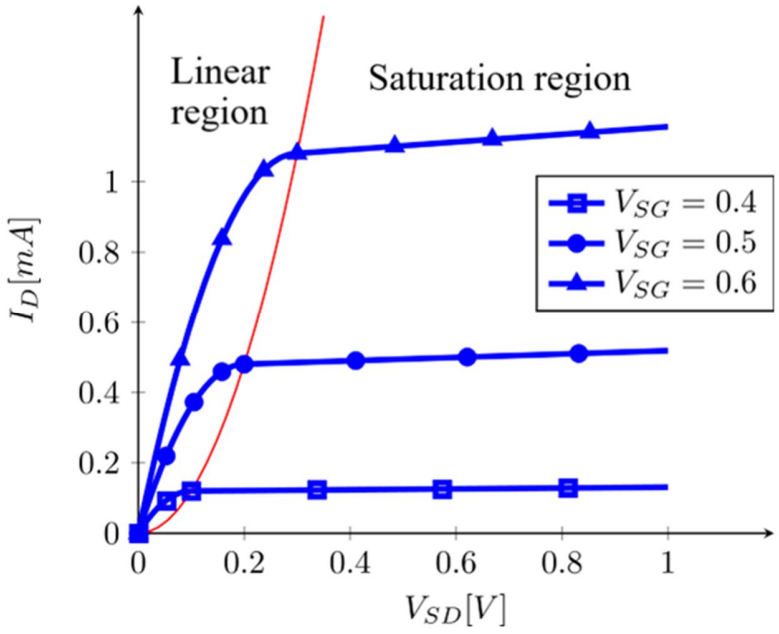

Figure 3 IV characteristics of NMOS transistor.

5. Experimental Setup and Procedure

The following practical experiments can be conducted on MOS transistors: IV characteristics measurement. Simple push-pull inverter characterization. Astable multivibrator characterization. Transmission gate switch characterization. The results of these experiments provide a good comprehensive understanding of the MOS technology.

The following equipment and apparatus are required to perform the experiments on MOS transistors: One MOS transistor N channel enhancement mode. One MOS transistor P-channel enhancement mode. One MOS transistor N channel enhancement mode (To drive small loads). Capacitors. Resistors. Variable resistor. Wires, connectors, bread-board, and IC prototyping board. Function generator. Digital Multi-Meter. Dual DC power supply. Oscilloscope. One PC with software installed.

All on-chip experimental setups should be powered with a battery or supply in the range of 5–15V. The power supply connections should be handled with care and preferably by connecting banana sockets to the boards. Before switching ON the power supply, verify the connections. Handle all the

spiced experimental setups with care. Prior to each experiment, the students should check the set of components and circuits for the experiment. Always check the condition of the wires and connectors before use. Minimum two sets of wires and connectors should be available for each experiment.

For experiments that need to be connected to a computer, first switch ON the CPU and the monitor. Then power ON the other instruments. After the instruments are ON, connect them to the PC. After setting up the experiment or the procedure for the experiment is done, the instruments should be properly disconnected and powered OFF. Handle the instruments with care and follow the instructions provided in the user manuals. Keep the laboratory neat and tidy. Arrange all the equipment and apparatus after performing the experiments. Always be cautious and aware of hazards while in the laboratory. Do not run, push, or shove in the laboratory. Students should not be in the laboratory without supervision by faculties or trained technicians.

Make sure that all gas and electrical appliances are switched OFF before leaving the laboratory. Ensure that all chemicals are returned to their proper storage places. Clear all spills immediately and report to the supervisor if any spill occurs. Do not block or tamper with any safety devices fitted to laboratory equipment. If any injuries occur, report them immediately to the supervisor. All work surfaces and sinks should be kept clear of personal belongings. Food, drink, and other such materials are strictly prohibited in the laboratory experimental areas.

Each experimental setup should be calibrated to achieve accurate results. Calibration is done by performing the procedures as specified in the user manuals or following the guidelines provided by the manufacturer. The basic setup of the instruments is checked to verify the proper functioning of the instrument. After the calibration, the experimental setup is verified with known commercial devices or experimental circuits. Verification is done to confirm that the setup has been calibrated properly and is capable of taking experiments with reasonable accuracy.

Assignments are given per experiment to the students, which consist of the theory of the experiment, procedure for the experiment and set of questions. The students should come prepared with the assignments for the experiment to be performed. It is essential to check the preparation of each student prior to the experiment to ensure that the experiments are conducted in an orderly manner and the time is effectively utilized. It is recommended that the students be divided into small groups with a maximum strength of five students per group. This helps keep the students active and involved in the experiments. Each group should maintain a separate manual to record the experiments with

results and observations. The group with maximum strength of students should perform the experiment first so that all the students get a chance to see and handle the required equipment and instruments.

6. Data Analysis and Interpretation

This section describes how the data obtained from the experiments are processed and interpreted to extract useful results.

7. Interpreting Results

In experiments involving the MOS transistor, it is conventional to plot relevant results on a graph, with one variable plotted against another. Here is explored how key results are affected by several important factors. These are important in order to contextualize what was found in the experiments. Results that are considered beyond the central four experiments may also be of relevance in understanding the effect of material properties on MOS transistor.

References

1. Winterfeld, H., 2019. On field-effect transistor concepts beyond traditional application.
2. Ahmad (Scholar) Bhat, T. & Mustafa (Guide), M., 2012. Simulation of FinFET Structures.
3. Tom, J., 2002. Analog IC Design and Fabrication.
4. Pearson, R., 1986. PMOS digital structures.
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MOS Transistors Practical Section

1. Target of the experiment

The objective of this laboratory activity is to understand the operation of MOS transistors through IV curves with the help of the Virtuoso simulator allows, on the one hand, to better understand the appearance of the IV characteristics of the transistor and, on the other hand, to study the influence of certain parameters (length L and width W of the gate, temperature T...) on these characteristics. While at it, this activity also aims to practice designers on what parameters should be altered to come up with a specific output (drain/source/current).

2. Procedure

If we start to apply a small voltage to the gate terminal (gate) of the MOS, a build-up of charges begins between the drain and source terminals. If we continue to gradually increase this voltage, the minority electrons in the substrate will begin to accumulate next to the insulator (SiO_2). This accumulation, due to the applied potential difference, will stratify into areas or layers with different electron concentrations. There will be a voltage value at which the electron accumulation is such as to form a conduction channel between drain and source terminals, which has not existed. This accumulation or layer of minority carriers is called investment layer. With the help of the software Virtuoso, we will simulate the characteristic curves of the MOS transistor, we will use the following circuit for this simulation.

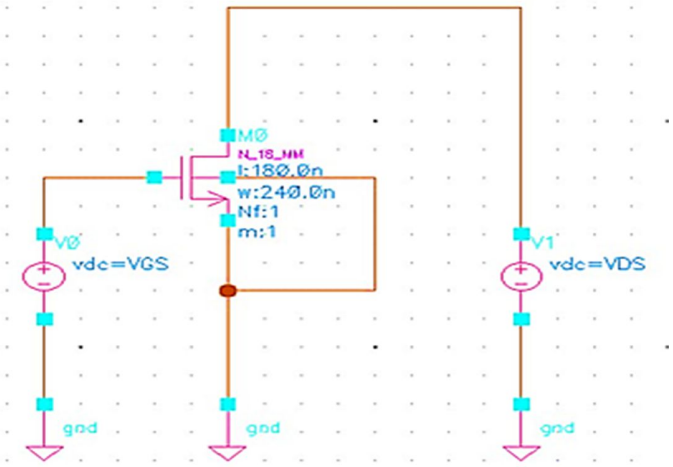
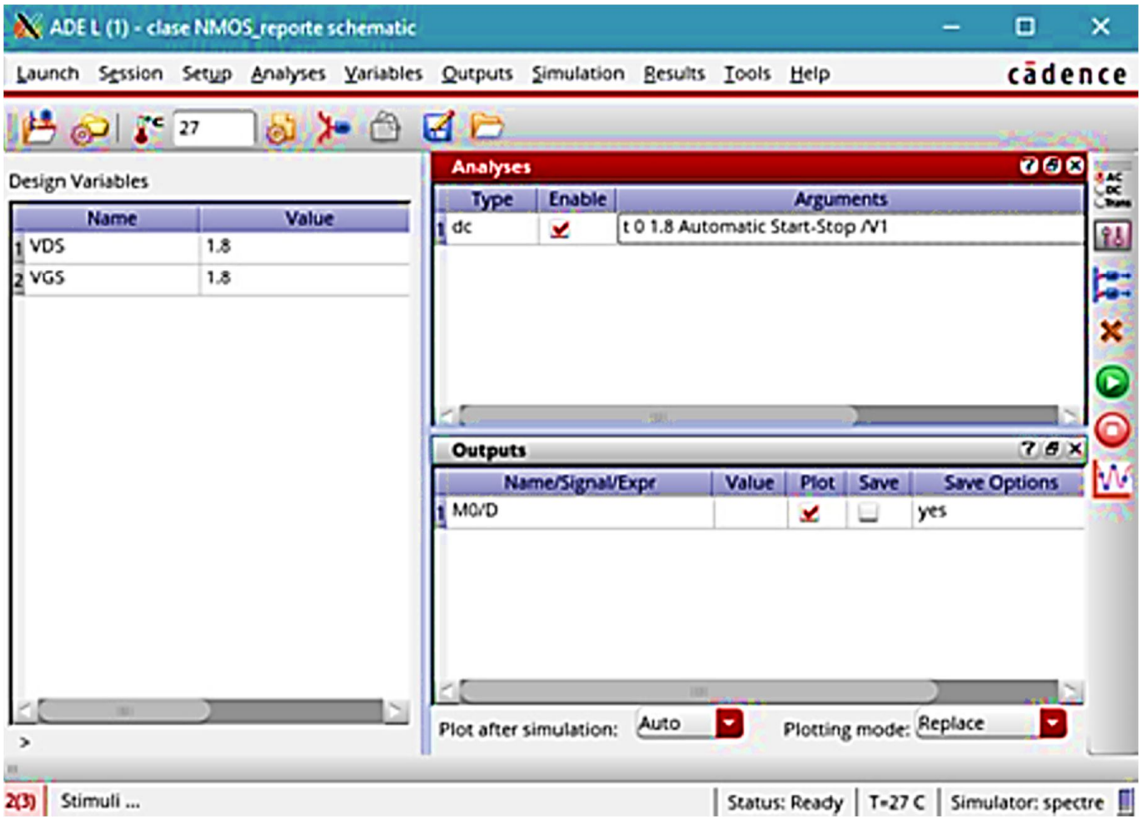


Figure 1 circuit developed for simulation.

<u>Step 1:</u> Characteristic curve I_{DS} *vs* V_{DS}

To be able to visualize this characteristic curve, we will carry out a simulation in DC, with the current Ids dependent on V_{DS}, in addition we will sweep the value of V_{GS} to obtain different curves and observe their behavior depending on the value of V_{DS}.

We will consider the voltages V_{DS} and V_{GS} as variables, the voltage V_{DS} as a sweep variable, and in the Parametric analysis option, we will select the voltage V_{GS} with a value between 0 and 1.8V. The output variable will be the I_{DS} current.



Furthermore, we consider the default values of the channel length of the MOS transistor (Figure 2).

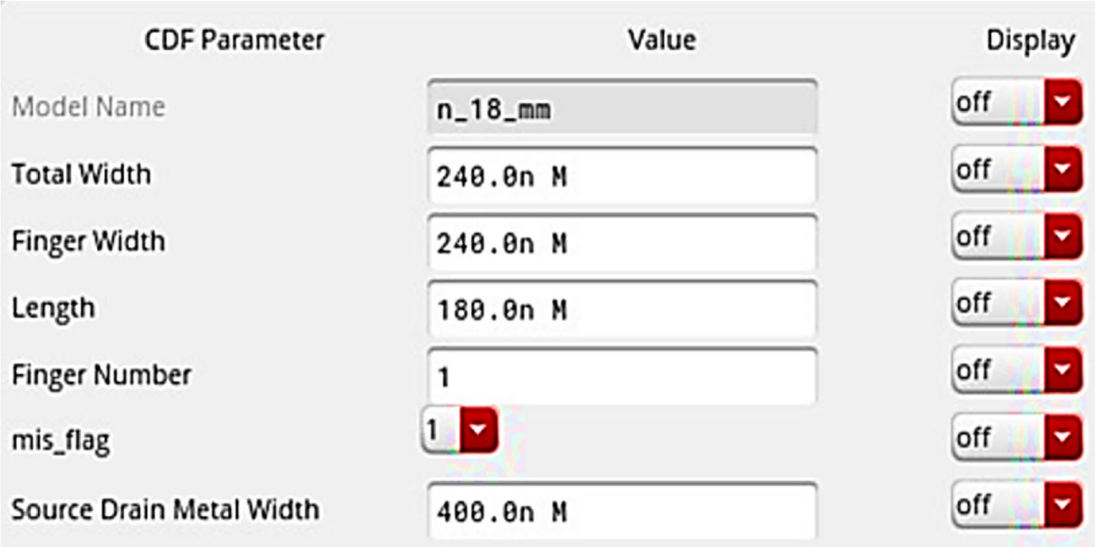


Figure 2 Default values for channel length.

The variation of I_{DS} via V_{DS} for some V_{GS} values, with default parameters of length channel is presented in Figure 3.

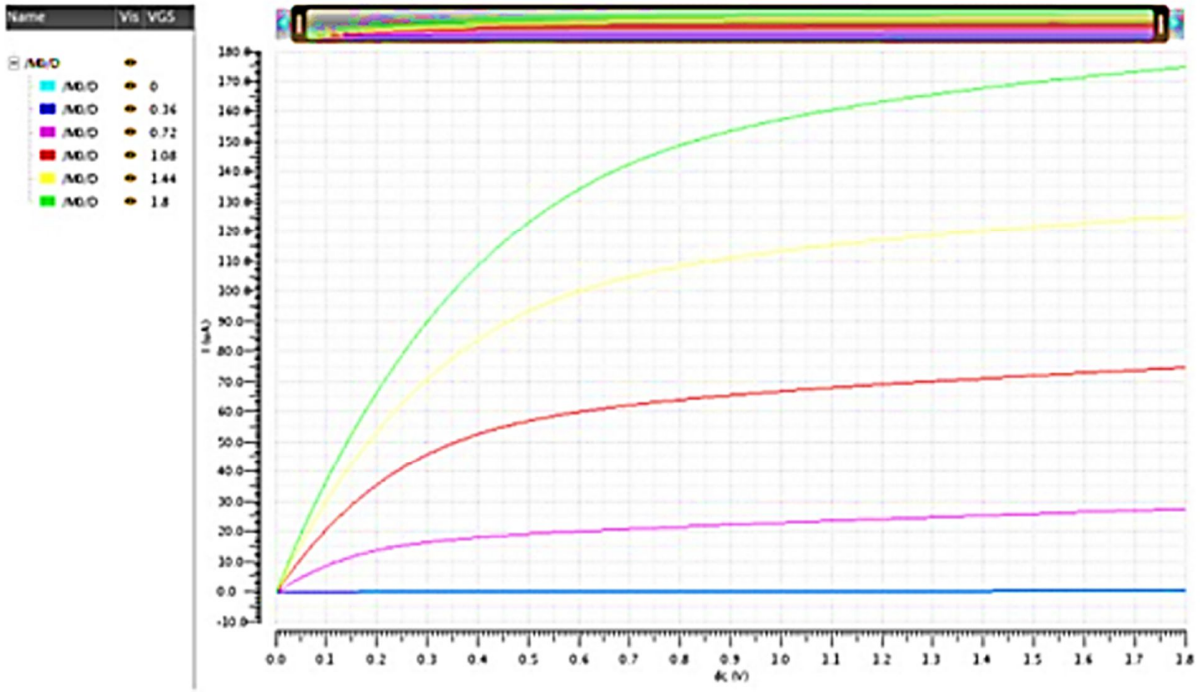


Figure 3 I_{DS} vs V_{DS} curve for some V_{GS} values, with default parameters of length channel.

We can see that the transistor has an upper percentage of the choked channel and depends on the depletion region, so the channel modulation effect is much greater. If we increase the length of

the channel, the percentage of throttling is lower, therefore, there is less dependence on the depletion region, having a flatter saturation region, as shown in Figure 4.

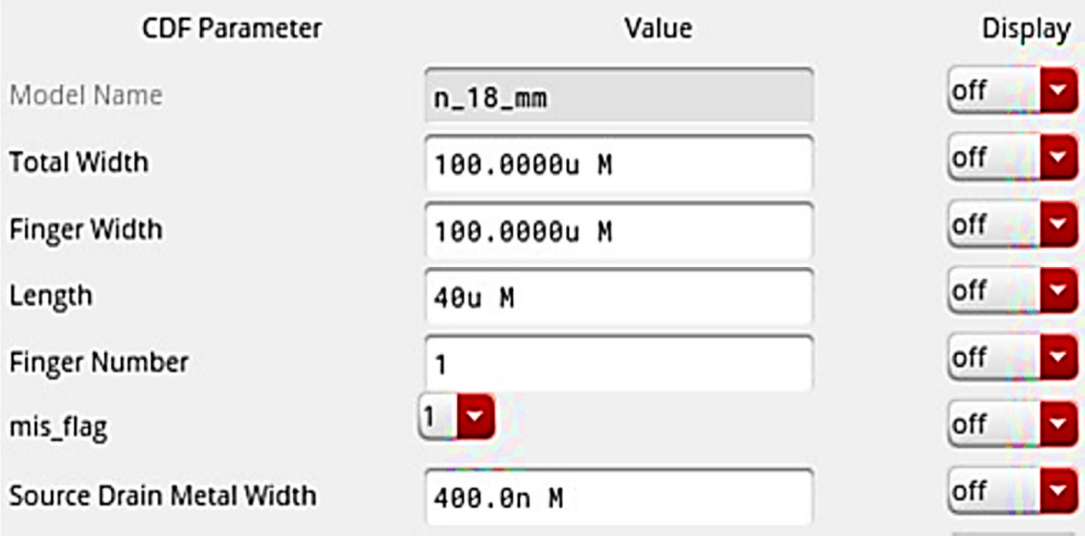


Figure 4 New length channel parameters.

The evolution of the curve I_{DS} *vs* V_{GS} for some V_{DS} values, with new parameters of length channel is illustrated in Figure 5.

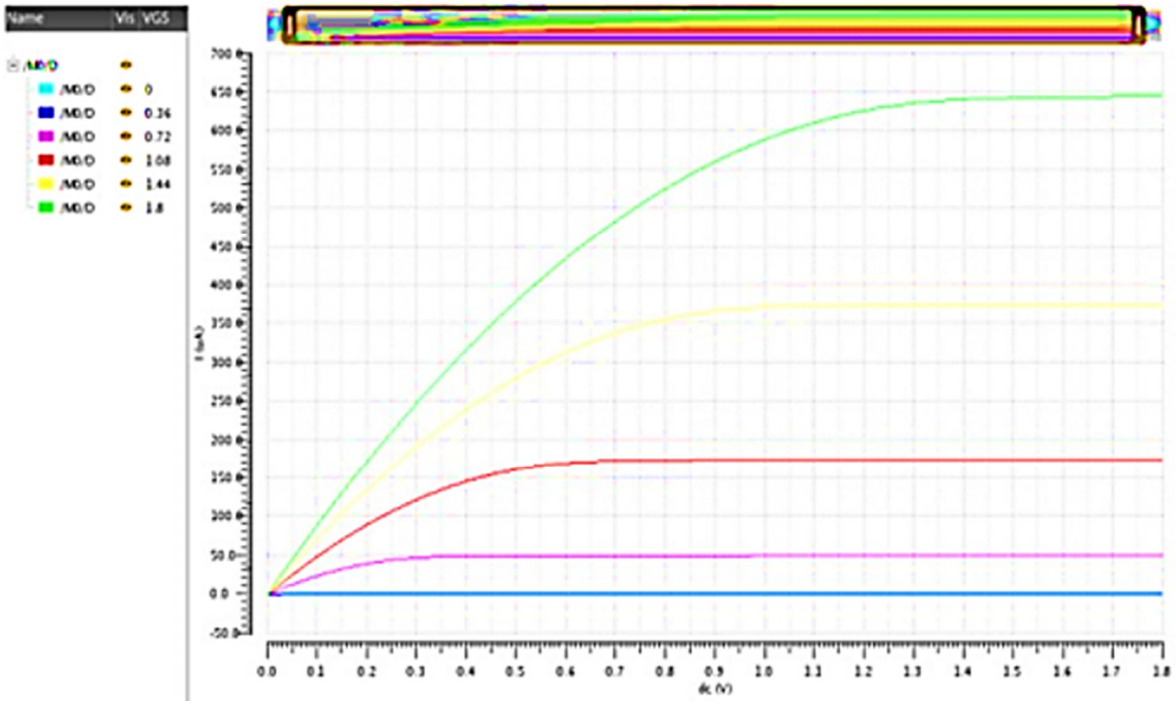


Figure 5 V_{GS} curve for some V_{DS} values, with new parameters of length channel.

<u>Step 2:</u> Characteristic curve I_{DS} *vs* V_{GS}

In this part, we will make the same steps as in the previous simulation. The difference is that the new variable to sweep will be V_{GS}, and in the parametric analysis option, we will choose the voltage V_{DS} in a range from 0 to 1.8V with a total of 6 steps, to obtain six curves. The I_{DS} *vs* V_{GS} curve with default parameters of the length channel is shown in Figure 6.

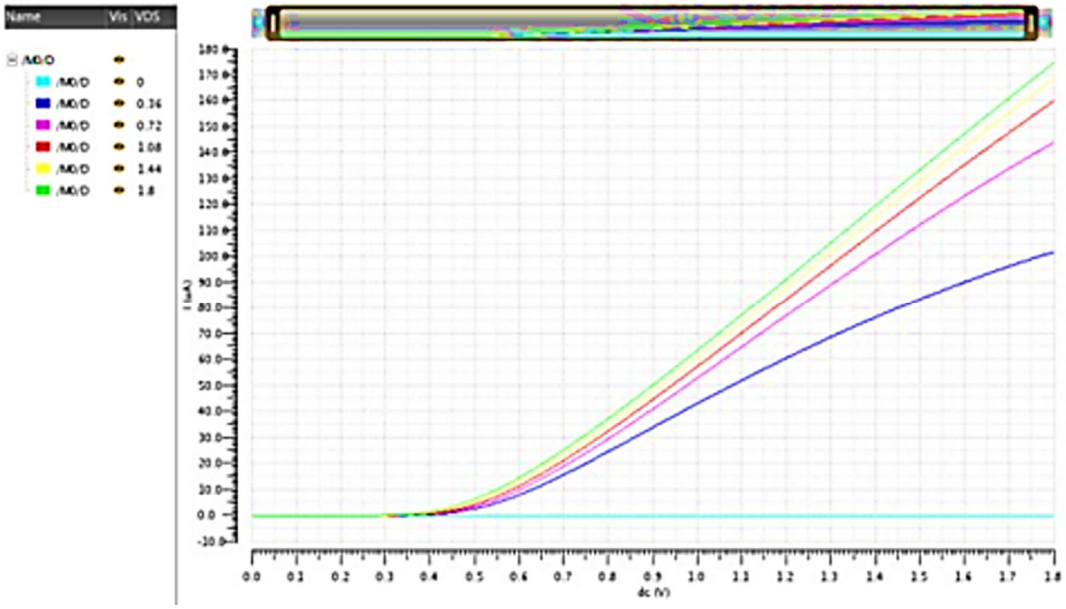


Figure 6 I_{DS} vs V_{GS} curve for some V_{DS} values, with default parameters of length channel.

If we increase the length of the channel, we obtain the next graphs (Figure 7).

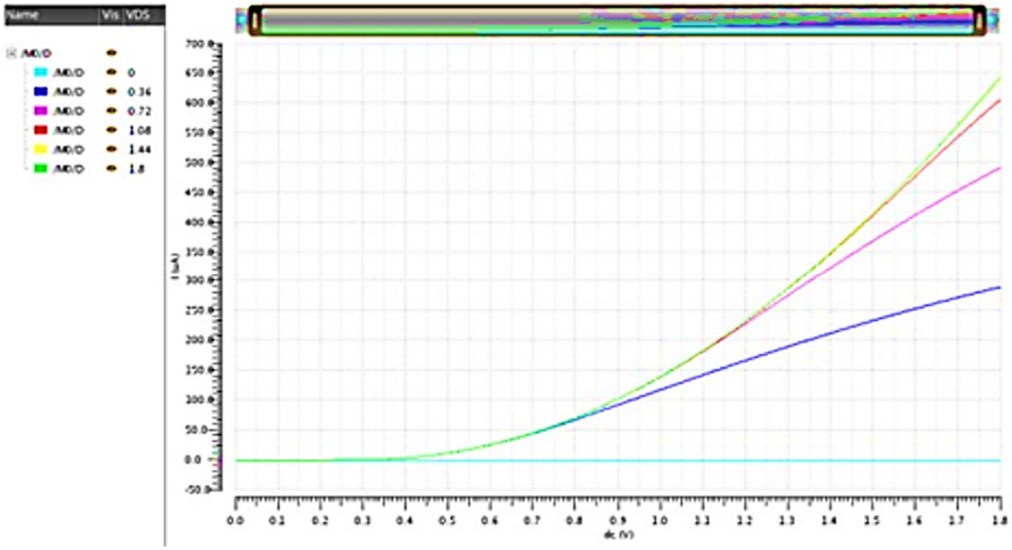


Figure 7 V_{GS} curve for some V_{DS} values, with new parameters of length channel.

We can see that, for both a small and a large channel length, the curves begin to slope when they exceed the threshold voltage V_{TH}. However, as the channel length increases, the slope of the curves is greater, which translates into higher transconductance. Disconnect the gate and drain of MOS then assign different values of V_{gs} to its gate terminal. Simulate the I_{ds} via V_{ds} characteristic curve.

With the scaling of the MOS transistors, unwanted effects begin to appear in the operation of these, known as short channel effects. As the channel length is shortened, the space-charge regions of the source and drain junctions will move closer together, beginning to interfere with the channel region, taking control of electrostatic phenomena from the gate. In saturation, a small increase in drain voltage will produce a small reduction in channel length. For devices with a very small channel, this effect becomes very important, so that the drain current is increased, appearing a slope in the saturation zone. Another effect produced occurs in the subthreshold region, which occurs when the voltage applied to the gate is less than V_{TH}. Under this condition, the MOS structure is in weak inversion and the current doesn't depend on the drain-source voltage, it depends on the gate-source voltage.

3. Analysis of results

- This activity introduced the basic operations of MOS through I-V curves. We noticed that by adjusting the effective channel dimensions of the MOS as well as the power supply to drive the device, one can adjust its drain-source current output. In addition to internal modifications of the device, one can also control the value of the drain-source current by applying a voltage drop from the gate of the device to the source. Confirmed by the result of this activity also is the fact that even if the gate-source voltage is set in the subthreshold region, the drain-source current is not actually zero but of a relatively small amount.
- The concepts and graphs presented in this report provide a basis to understand operation of the MOS transistor and thus be able to model its behavior and use it in various applications, since it is one of the most used elements in analog and digital electronics. We can conclude that the graphs obtained with the data shown agree with what is expected in the theory about the behavior of the MOS transistor.
- When the drain voltage is small (Linear region), the resistance of the channel will remain constant, so it's to be expected that the current-voltage characteristics I_{DS} vs V_{DS}, when varying the gate voltage, will be practically linear.

➢ Saturation region. With increasing (Saturation region) voltage on the drain, the effective voltage to maintain inversion, as well as the drain, will start to increase. As a result, the channel resistance will increase. Thus, the characteristic curve will start to curve downward, as shown in the Figure 8.

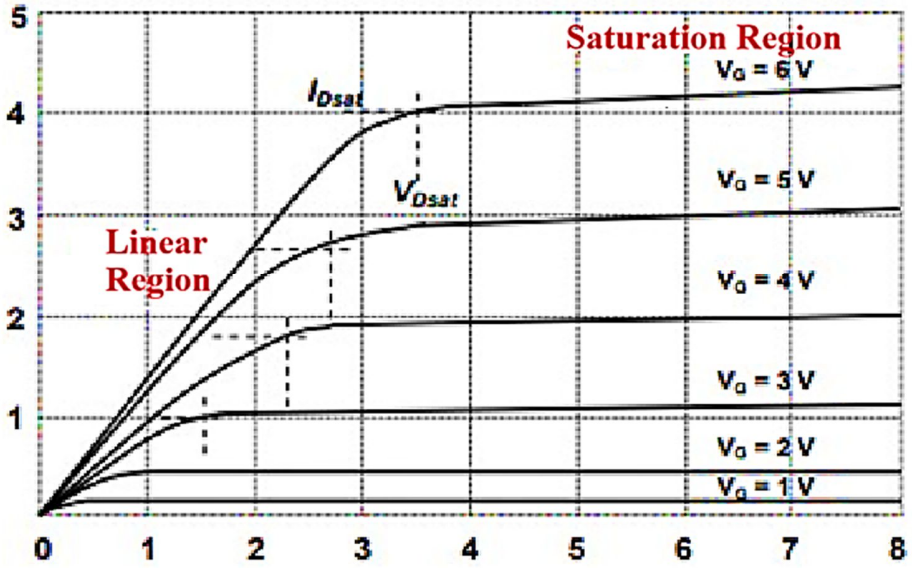


Figure 8 Current Voltage characteristics of a MOS transistor.

Questions / Discussions:

1) If we increase the length of the channel, what changes will occur to its corresponding curve?

The curve increases its slope. There will be a slight increase in the V_{th} but the noticeable increase is in the I_{ds} as channel length is increased.

2) What is the relationship between the channel length and the slope of the curve in Step 2?

The channel length is inversely proportional to the slope of the resulting curve. This means that as the length is increased, there is a visible decrease in the curve's slope, which also results to a decreased value of I_{ds}.

3) When the MOSFET operates in subthreshold region, what is the relationship between Vgs and the slope of the curves in Step 2? What device, either PMOS or NMOS, has the larger slope? Why?

By testing, that is by altering the values of V_{gs} in the subthreshold region, there is no changes in the way the curve looked. This can be explained by the fact that in the curve, V_{gs} is the independent variable of I_{ds}. This means that no changes in V_{gs} will affect how the I_{ds} curve will look, V_{gs} will just generate a value of I_{ds} that will follow the given curve. Therefore, there is no relationship between V_{gs} and the slope of the curve. On the other hand, NMOS has a larger slope compared to PMOS because NMOS has higher electron mobility than PMOS which has a lower hole mobility and transconductance.

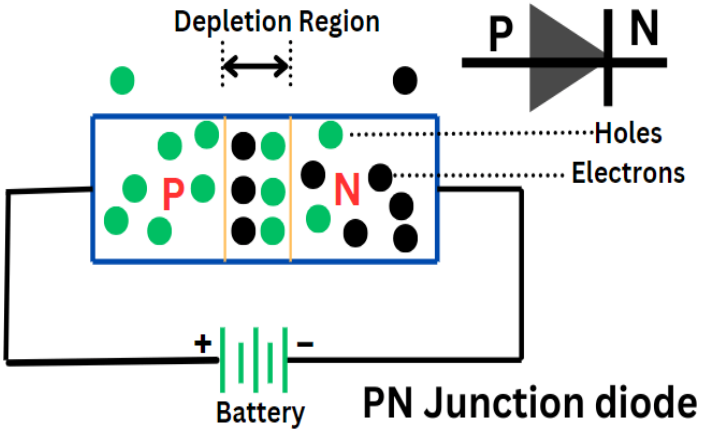
4) Explain how MOSFET functions?

When there is no voltage on the gate, the channel exhibits its maximum conductance. As the voltage on the gate increases (either positively or negatively, depending on whether the channel is made of P-type or N-type semiconductor material), the channel conductivity decreases.

Practical Works 05

Diode junction applications

L3 physics of materials



By Dr. GACEM Amel

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Diode Junction Application — Practical Section

1. Introduction

We know that a Diode allows the current flow only in one direction and hence it acts as a one-way switch. Diode is made of P and N type materials and has two terminals namely anode and cathode. This device can be operated by controlling the voltage applied to it. When the voltage applied to the anode is positive with respect to the cathode, the diode is forward biased. If the voltage applied to the diode is greater than the threshold level (generally it is of 0.6V), then diode acts as a short circuit and allows the current flow. If the polarity of the voltage is changed that means cathode is made positive with respect to anode, then it is reverse-biased and acts as open circuit results no current to flow. The application areas of diodes include communication systems as limiters, clippers, gates; computer systems as logic gates, clampers; power supply systems as rectifiers and inverters; television systems as phase detectors, limiters, clampers; radar circuits as gain control circuits, parameter amplifiers, etc. The following description describes the various applications of diodes briefly.

2. Definition

A diode junction is another name given to the crystal PN. The word diode is the contraction of say (two) and electrodes. They are made from semiconductors by joining two parts: one doped P, the other doped N (Figure 1(a)). Their physical operating principle is used in many active components in electronics (transistors, etc.). An ordinary resistor is a linear component, its current/voltage characteristic IV, is a straight line:

$$V=RI$$

For the diode it's different, it's anon-linear component, its characteristic is not a straight line (Figure 1(b)). The potential barrier, electrically represented by a threshold voltage V_S, is the cause: if the voltage across the diode is $< V_S$, the current is low and equal to the saturation current noted I_S; when the voltage across the diode is $> V_S$, the current through the diode increases rapidly and follows the equation:

$$I_D = I_s\left[exp\left(\frac{e.V_D}{KT}\right) - 1\right] \approx I_s \cdot exp\left(\frac{e.V_D}{KT}\right) = I_s \cdot exp\left(\frac{V_D}{V_T}\right)$$

V_D is the voltage across the diode, I_S is the diode saturation current or reverse current, $V_T = KT/e$ is the thermal voltage equal to 25 mV at T=20 °C (293 K); K is Boltzmann's constant.

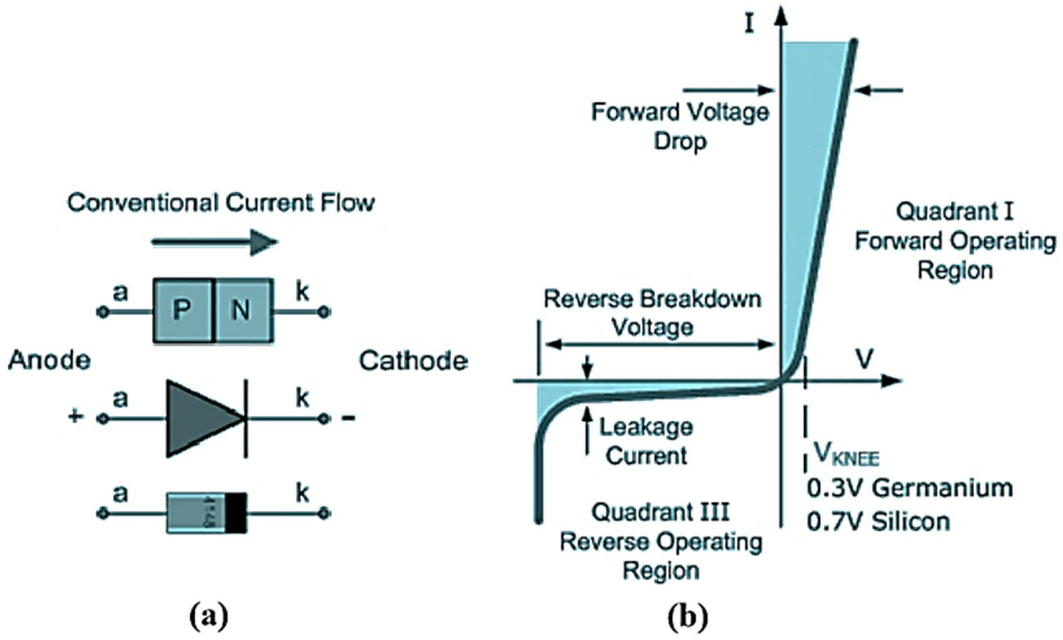

Figure 1 PN junction configurations and Characteristics.

3. Basic Principles

To solve a diode circuit, you need to know the state of the diodes (conducting or blocking) to replace them with their equivalent models. However, the state of a diode clearly depends on the voltage values (V_D) and current (I_D) which are applied to it: passing diode if $V_D > Vs$ And $I_D > 0$ and blocking diode if $V_D < Vs$ And $I_D = 0$. So we go around in circles: without knowing the state of the diode we do not know how to solve the circuit and without having solved the circuit, we do not know the state of the diode. To break this vicious circle, we must use reasoning by hypothesis:

- ✓ Pose a hypothesis.
- ✓ Reason as if this hypothesis were correct.
- ✓ Check whether the result obtained at the end of this reasoning is compatible with the initial hypothesis.

For each diode, there are only two possible (and mutually exclusive) hypotheses: either it is passing : $V_D > V_s$ (or zero for ideal diode) and $I_D > 0$, either it is blocking : $V_D < V_s$ (or zero for ideal diode) and $I_D = 0$. The working principle of a diode circuit is based on the biasing conditions of diodes. When a diode is forward biased, a small voltage is applied such that the p-type semiconductor's positive charge is made more positive than the n-type. This reduces the width of the depletion zone, allowing electrons from the n-side and holes from the p-side to flow across the junction. The diode then acts like a closed switch. In contrast, reverse biasing a diode makes the n-type more positive than the p-type. As a result, the depletion zone widens, blocking the flow of charge carriers. The diode behaves as an open switch. Diode circuits utilize this asymmetric conduction in innovative ways for various applications (Figure 2).

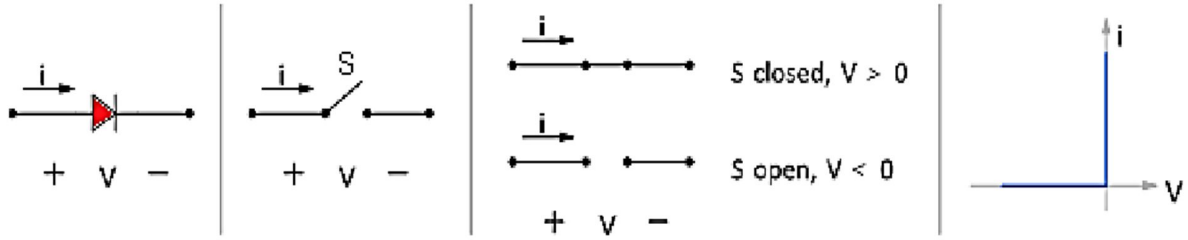

Figure 2 Characteristics of an ideal pn junction diode.

4. Some Common Applications of Diodes

Diode junction applications have become an integral part of modern electronic devices, often going unnoticed by users. There are various different types of applications of diodes, the most common are: Rectifiers, Clipper Circuits, Clamping Circuits, Reverse Current Protection Circuits; In Logic Gates, Voltage Multipliers, and many more. Now let us understand each of these applications of diodes in more detail. Most electronic systems (TV, computers, ...) need an almost perfect direct voltage to function. However, the voltage provided by the electrical network is alternating (sinusoidal), so it is necessary to transform this alternating voltage (AC) into direct voltage (DC). This is achieved by a simple power supply successively performing the following operations: lower the level of the alternating voltage by a transformer, rectify the lowered voltage by removing the negative alternations (single-wave rectifier**)** or by transforming them into positive alternations (full wave rectifier). This operation of recovery uses diodes which operate with currents ranging from 1 to 10 A and voltages ranging from 50 to 3000 V, filter and smooth the rectified voltage and regulate to obtain a typical DC voltage.

<u>Step 1:</u> Diode as a Rectifier

The most common and important application of a diode is the rectification of AC power to DC power. Using the diodes, we can construct different types of rectifier circuits. The basic types of these rectifier circuits are half wave, full wave center tapped and full bridge rectifiers. A single or combination of four diodes is used in most of the power conversion applications. Below figure shows diode operation in a rectifier (Figure 3). The following figure illustrates half-wave rectification. A transformer is often used to couple the sinusoidal AC voltage to the rectifier. Transformer coupling provides two advantages: first, it provides a step-down or step-up effect on the input voltage

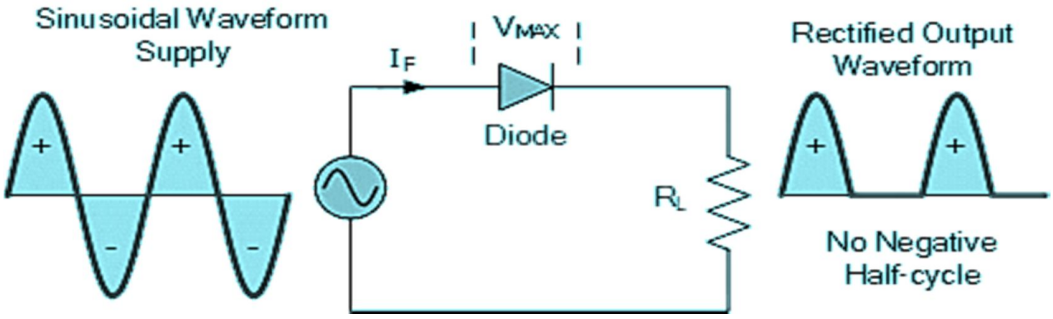

Figure 3 Diode as a rectifier.

We will consider the diode as perfect, in this case if it conducts we will have V_{AK}=0V and V_s=V_e, this happens for $I_D > 0$ so for $I_D = V_s/R = V_e/R > 0$ or $V_e > 0$. For negative alternations ≤ 0,the diode is blocked, I_D=0, $V_S = 0$ and $V_{AK} = V_e$. We obtain the following chronograms (Figure 4).

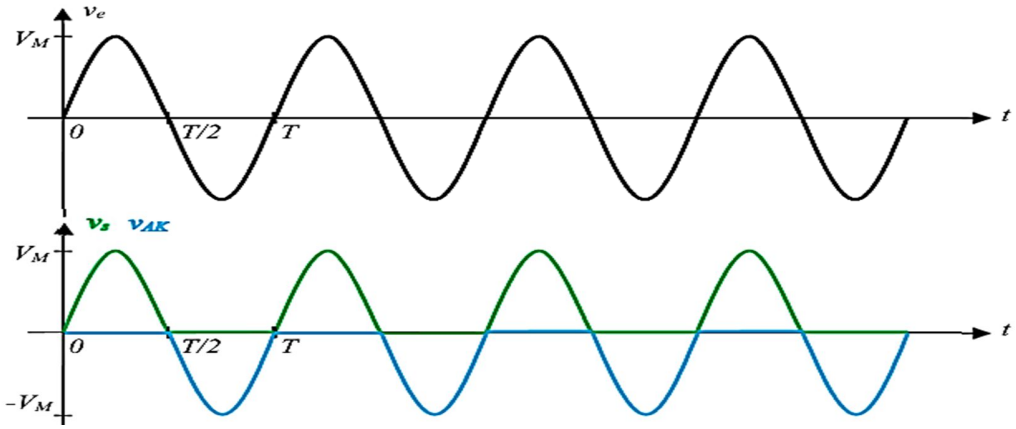

Figure 4 Chronograms of diode rectifier circuit.

The average value of v_s is given by:

$$v_{smoy} = \frac{1}{T}\int_0^T v_s dt = \frac{1}{T}\int_0^{\frac{T}{2}} V_M sin\omega t \, dt$$

Either:

$$v_{smoy} = \frac{V_M}{\pi}$$

The effective value of v_s is :

$$v_{seff} = \sqrt{\frac{1}{T}\int_0^T v_s^2 dt} = \sqrt{\frac{1}{T}\int_0^{\frac{T}{2}} V_M^2 sin^2\omega t \, dt}$$

Where:

$$v_{seff} = \frac{V_M}{2}$$

The average power dissipated in the resistor is defined by:

$$P_{moy} = \frac{1}{T}\int_0^T v_s i_D dt = \frac{1}{T}\int_0^{\frac{T}{2}} \frac{V_M^2 sin^2\omega t}{R} \, dt$$

Either:

$$P_{moy} = \frac{V_M^2}{4R}$$

<u>Step 2</u>: Two diodes rectifier

Full-wave rectification with a mid-point transformer and two identical voltage sources (called a "midpoint" voltage source). The assembly used is that of the Figure 5.

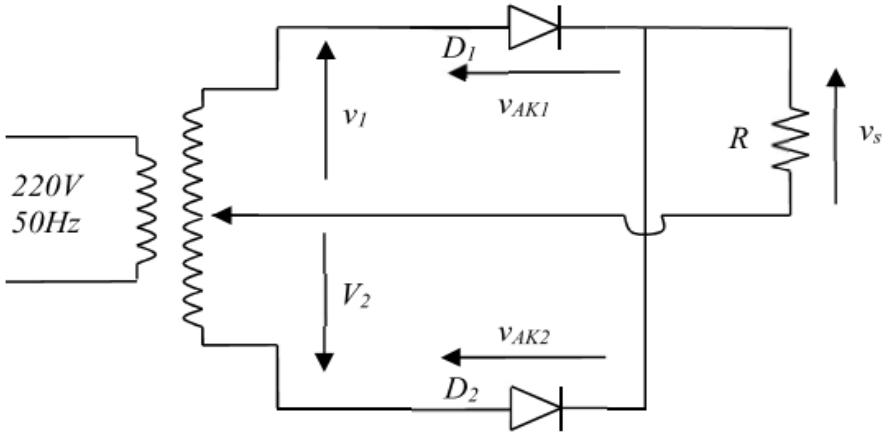

Figure 5 Two diode as rectifiers.

The tensions $V_1$and V_2 are in phase opposition $V_1=-V_2=V_M \sin(-t)$. During the positive alternation of V_1, $0 < t < T/2$, the tension V_2 is negative. The diode D_1will therefore drive and the diode D_2 gets stuck and $V_s=V_1= V_M \sin(-t)$ and $V_{AK2}=2V_2$. During the negative alternation of V_1, $T/2 < t <T$, the tension V_2 is positive. The diode D_2 will therefore drive and the diode D_1 gets stuck and $V_s = V_2= -V_M \sin(-t)$ and $V_{AK1} = 2V_1$. Therefore the voltage collected at the terminals of R has two alternations of the same sign. We obtain the timing diagrams shown in the Figure 6.

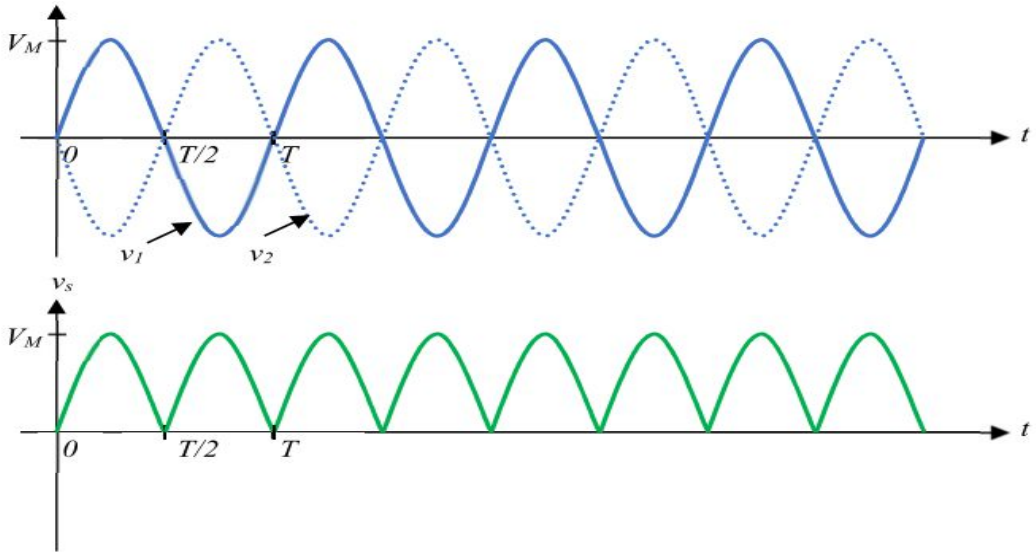

Figure 6 Chronograms of diode rectifier circuit.

The average value of Vs is given by:

$$v_{smoy} = \frac{1}{T}\int_0^T v_s dt = \frac{2}{T}\int_0^{\frac{T}{2}} V_M sin\omega t \, dt$$

Thus:

$$v_{smoy} = 2\frac{V_M}{\pi}$$

The average power dissipated in the resistor is defined by:

$$v_{seff} = \sqrt{\frac{1}{T}\int_0^T v_s^2 dt} = \sqrt{\frac{2}{T}\int_0^{\frac{T}{2}} V_M^2 sin^2\omega t \, dt}$$

Either:

$$v_{seff} = \frac{V_M}{\sqrt{2}}$$

The average power dissipated in the resistor is defined by:

$$P_{moy} = \frac{1}{T}\int_0^T v_s i_D dt = \frac{2}{T}\int_0^{\frac{T}{2}} \frac{V_M^2 sin^2\omega t}{R} \, dt$$

Where:

$$P_{moy} = \frac{V_M^2}{2R}$$

Step 3: Four diode rectifier (Graetz bridge)

The circuit of Figure 7 is similar to the previous one in that it outputs a voltage rectified double alternation. It does, however, require four diodes connected in a bridge at the output of the secondary circuit of a transformer.

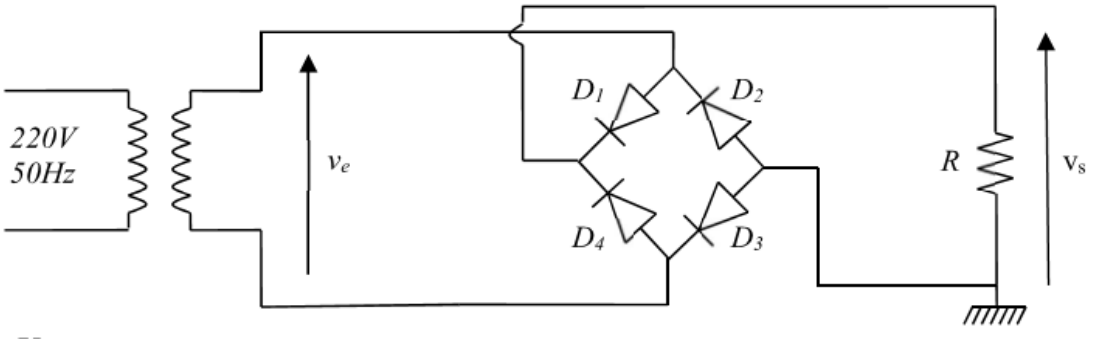

Figure 7 Four diode rectifier.

During the positive alternation of Ve ($V_e > 0$) the current will have the same direction as that indicated for the voltage V_e, diodes $D_1$and D_3 will therefore drive and the diodes D_2 and D_4 are blocked. We will therefore have $V_s = V_e > 0$. During the negative alternation of V_e ($V_e < 0$) the current direction will be the opposite of that indicated for the voltage V e, diodes D_2 and D_4 will therefore drive and the diodes $D_1$and D_3 are blocked. We will therefore have Vs = -Ve > 0.

The input voltage is:

$V_e = V_M \sin(-t$ Therefore the voltage collected at the terminals of R has two positive alternations. We obtain the diagrams presented in the Figure 8.

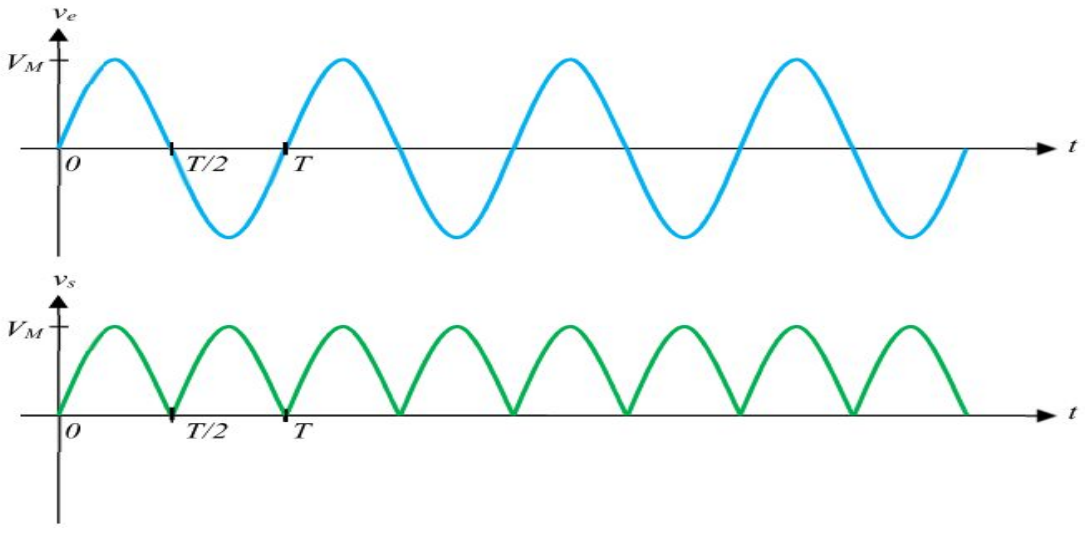

Figure 8 Chronograms of diode circuit.

We will have:

$$v_{smoy} = 2\frac{V_M}{\pi} \; ; v_{seff} = \frac{V_M}{\sqrt{2}} \text{ and } P_{moy} = \frac{V_M^2}{2R}$$

<u>Step 4:</u> Filtering the rectified voltage

The rectified signal has a DC component and an AC component called ripples. Several filtering methods are used to remove the ripples and get as close as possible to a DC voltage. The simplest method is to place a capacitor of capacitance C_{in} parallel with the resistance load R as shown in the following Figure 9.

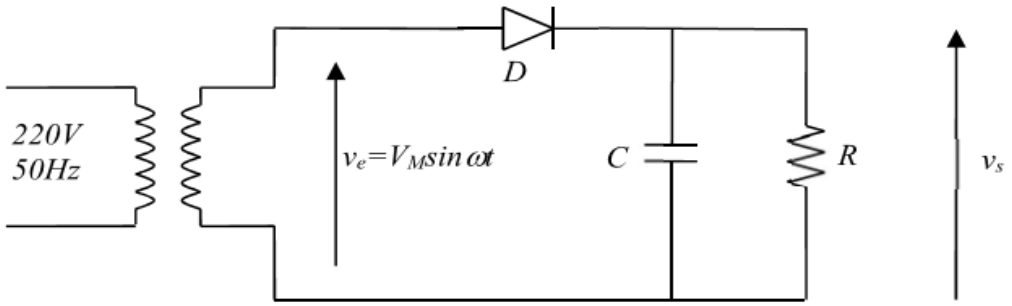

Figure 9 Filtering the rectified voltage circuit.

During the half of the positive alternation of Ve, the diode is conductive, C charges, at t = T/4, $V_e = V_M$ and the capacitor charge is maximum $Q_{max} = CV_M$, after this moment the diode becomes reverse biased, the capacitor discharges into the resistor R. If the time constant τ= RC of the circuit is weak in front of the period T of the signal V_e, the capacitor discharges completely before V_s increases again (Figure 10).

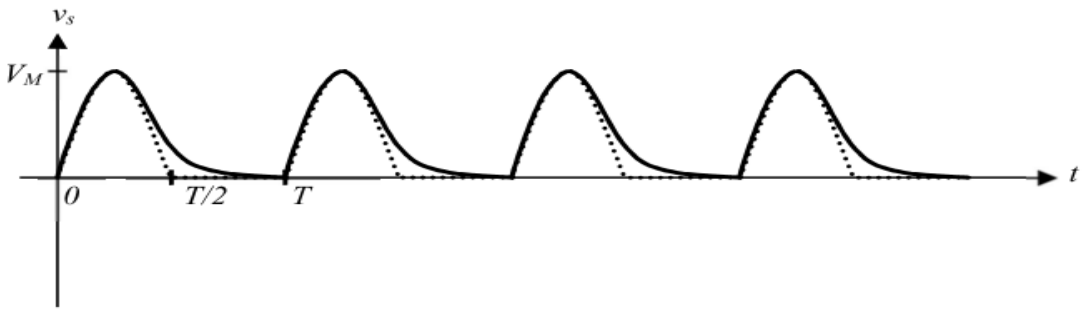

Figure 10 Chronograms of diode circuit.

If the time constant RC is big in front T, the capacitor discharges very slowly and at the limit Vs remains practically equal to V_M. We then collected at the output an almost continuous filtered voltage of ripple $\Delta V_s = V_{smax} - V_{smin}$ (Figure 11).

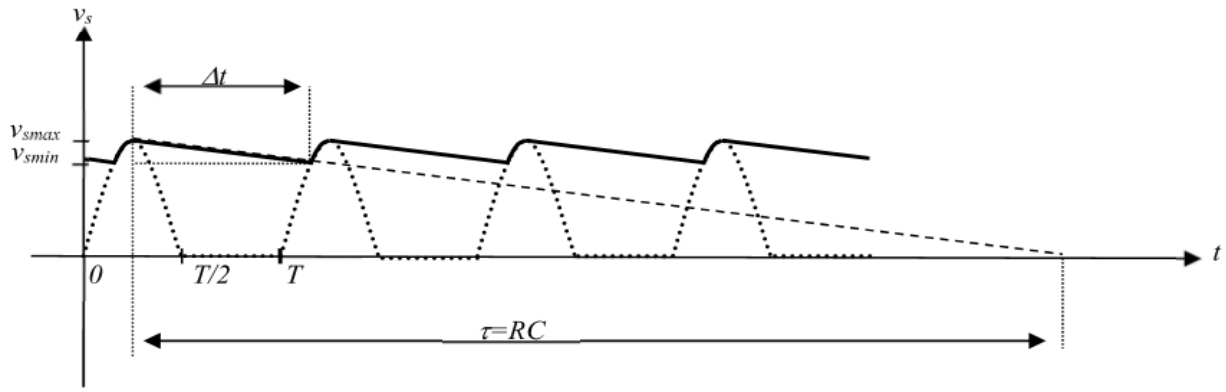

Figure 11 Chronograms of filtered circuit.

The output voltage is all the closer to V_M that RC is bigger in front T. The variation of V_s is exponential and follows the tangent to the origin of the capacitor discharge. The value of capacity C is given using triangles similar:

$$\frac{v_{smax}}{RC} = \frac{\Delta v_s}{\Delta t}$$

Where, V_{smax}: maximum voltage value V_s. ΔV_s: ripple that we impose on ourselves when studying power supplies $\Delta V_s << V_{sma}$. Δt :capacitor discharge time ($\Delta t \approx T$ due to the very wide tolerances of the filter capacitors). R is equivalent resistance to the load which can be defined by the relation:

$$R = \frac{v_{smoy}}{I_{moy}} \approx \frac{v_{smax}+v_{smin}}{2I_{moy}} = \frac{v_{smax}\ \frac{\Delta v_s}{2}}{I_{moy}}$$

I_{moy} is the average current supplied by the capacitor during discharge .So we can generalize: for a frequency of 50Hz and $T = 210^{-2}$ s, the capacity C is:

Simple alternance:

$$C \approx \frac{v_{smax}.2.10^{-2}}{R.\Delta v_S}$$

Double alternance:

$$C \approx \frac{v_{smax}.10^{-2}}{R.\Delta v_S}$$

<u>Step 5:</u> Zener regulator

The Zener diode is called voltage regulator diode, because it maintains an almost constant voltage at its terminals V_Z despite variations in the current flowing through it. In normal operation, it is reverse polarized with resistance R_{in} series for current limitation. If we want to determine the reverse Zener current in the diode, we will have:

$$V_R = V_S - V_Z \;\rightarrow\; I_S = \frac{V_R}{R} = \frac{V_S - V_Z}{R}$$

Where, I_S which must be less than I_{max}. In regulation, the Zener diode is used at the output of a power supply (transformer + rectifier + filtering) to obtain a continuous voltage lower than that given by the power supply: it is a Zener voltage regulator or simply Zener regulator (Figure12).

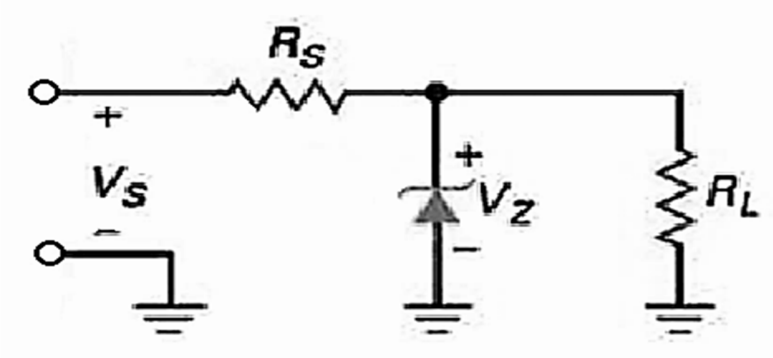

Figure 12 Circuit of Ziner diode.

The series current through the resistor R is given by :

$$I_S = \frac{V_R}{R} = \frac{V_S - V_Z}{R}$$

This current remains the same, whether the load is present or not, always equal to the voltage across the resistor divided by the resistance.

Theoretically, the voltage across the load is equal to the Zener voltage because R_L is in parallel with the diode. We therefore have: $V_L=V_Z$, which gives:

$$I_L = V_L / R_L = V_Z / R_L$$

The Zener Current is obtained with Kirchhoff's law:

$$I_S = I_Z + I_L \Rightarrow I_Z = I_S - I_L$$

5. Interpreting Results

This exploration of the practical experience of applying diode junctions has revealed that despite their small size, they are an essential part of electronics because they make it work. They come in many shapes and sizes and have many different applications. It is also important to understand the different types of diodes; such as rectifier and Zener diodes. Diodes are one of the most common components of power supplies, from AC to DC conversion to ripple reduction and regulation, all of this is achieved by diodes. which are not only power supplies, they are one of the main building blocks of communication systems. It is the basis of amplitude modulation, where audio current is sent to the diode with a high frequency carrier signal; the diode demodulates it, which produces an audio output. Understanding the practical experience is directly related to everyday life and the simple operation of everyday things. Due to their versatility and adaptability, diodes can be adapted to almost any application possible or under development.

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Diode Junction Application Practical Section

1. Instrumentation and simulation

PSIM (Physical Security Integration Management) software is a simulation software that can be used in general electricity, electrical engineering and electronics (analog, logic). The demo version allows us to tackle the problems we have to tackle The following figure shows typical screen display of PSIM environment.

In the Figure 1, to illustrate as examples, two PSIM circuit files are open: a boost power factor correction circuit and a dc-dc buck converter circuit.

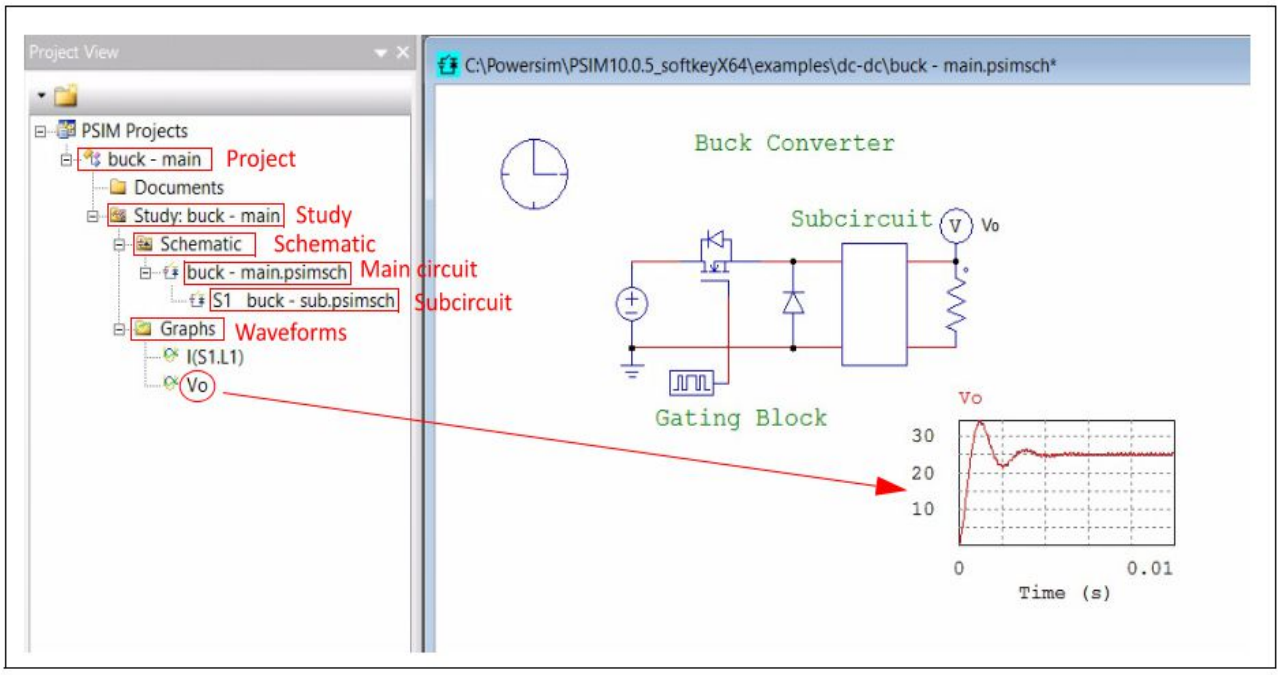

Figure 1 Buck converter example.

2. Principle and Working

The diode is a electronic component. It's a dipole non-linear and polarized (or not symmetrical). The direction of connection of a diode therefore has an importance on the operation of

the electronic circuit in which it is placed. In this practical work we will use two types of diode: Rectifier diode and Zener diode.

3. Target of the experiment

Study of the "signal diode" component alone, its external characteristic $I_d=f(V_d)$, and its use in single diode, four diode or Greatz bridge rectifier assemblies. Similarly, we study the "Zener" diode and visualize its characteristic $I_z=f(V_z)$ in the forward and reverse directions.

4. Results and discussion

Step 1: Rectifier diode

Using the PSIM software, we create the circuit above (Figure 2), where the alternating voltage source has an amplitude of 8V and a frequency of 100Hz.

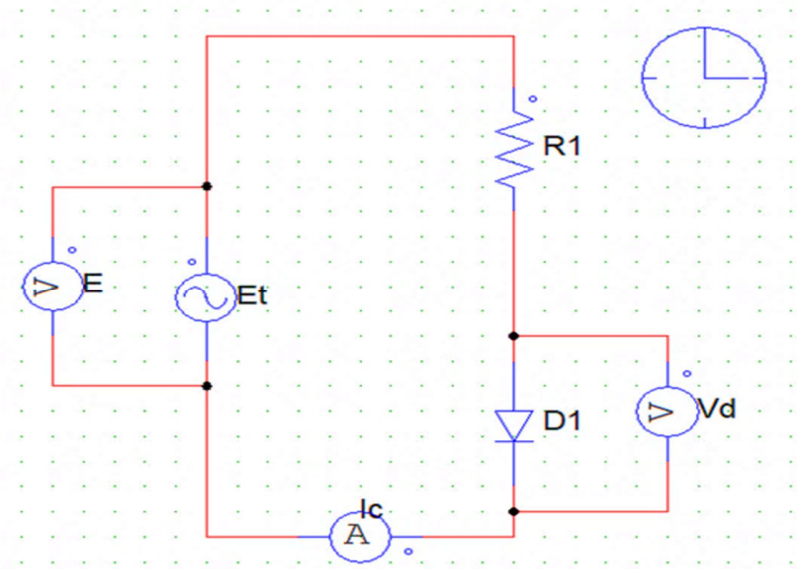

Figure 2 Rectifier diode circuit.

Visualization of the signals e(t) of the source and the voltage across the diode $V_d(t)$ is presented in Figure 3 and 4.

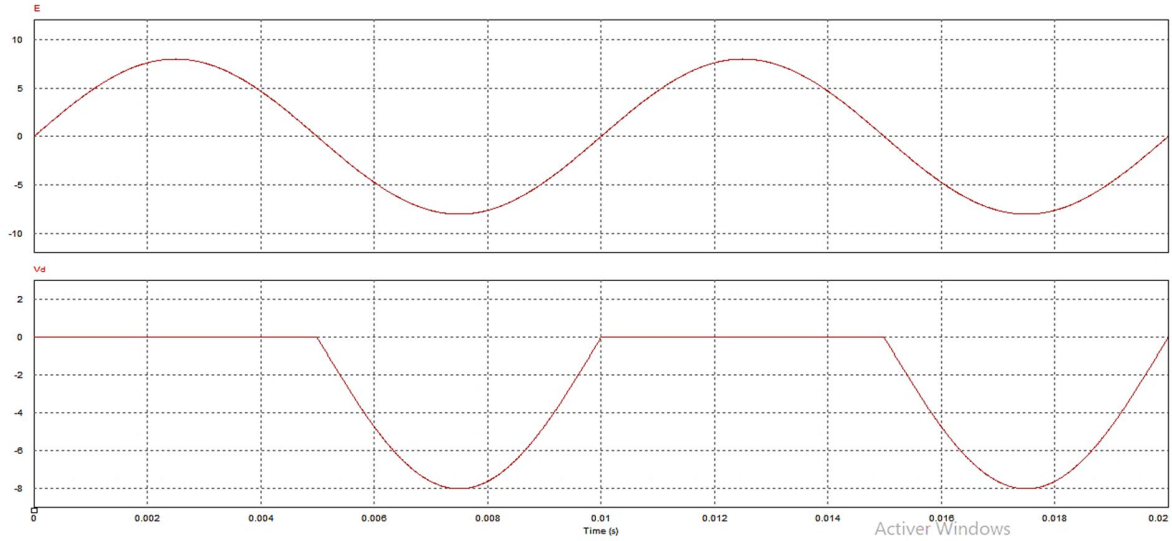

Figure 3 Variation of e(t) and V_d(t) as a function of time.

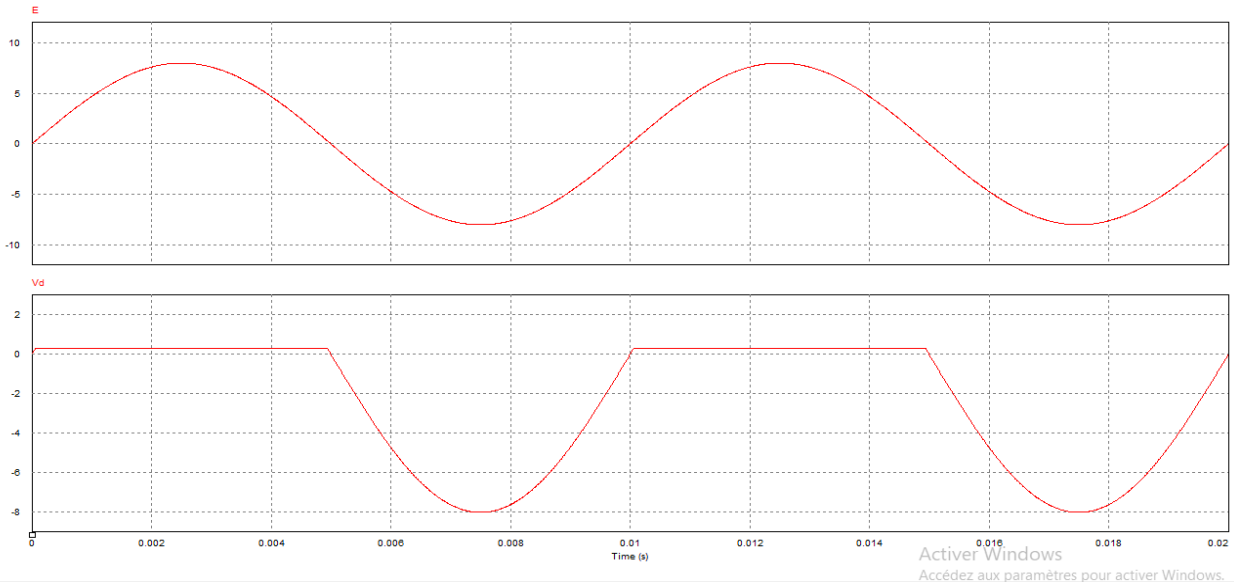

Figure 4 Variation of e(t) and V_d(t) as a function of time with 'Forward Voltage'=0.3V.

We note that:

The voltage of the AC source does not change over time. Concerning the voltage at the terminal of the diode, V_d is zero throughout the positive alternation so we can say that the diode is blocked, and conducting in the negative alternation. With the 'Forward Voltage' option we notice that there is an increase of 0.3V in the voltage value at the diode terminal throughout the positive half cycle.

The role of this option:

Indicates the voltage value that will pass through the diode, if the current passes in the forward direction when V_d is greater than Vseuil the diode becomes conductive.

- ✓ **The maximum value of the current in the assembly I_{max}**

$$e = E_{max} \Rightarrow i = I_{max} \qquad e = R.i + V_s$$

$$I_{max} = \frac{E_{max} - V_s}{R}$$

$$I_{max} = \frac{8 - 0.3}{100} = 0.077A$$

- ✓ **The shape of these two signals over a period:**

In the positive direction $v_e(t) > V_s$, therefore the diode becomes conductive and if $0 < v_e(t) < V_s$, thus the diode becomes blocked.

In the negative direction if $v_d(t) < V_s < 0$, the diode becomes blocked therefore $i(t) = 0$ and if $v_e(t) < V_d$, the diode becomes conducting thus $i(t) > 0$ (Figure 5).

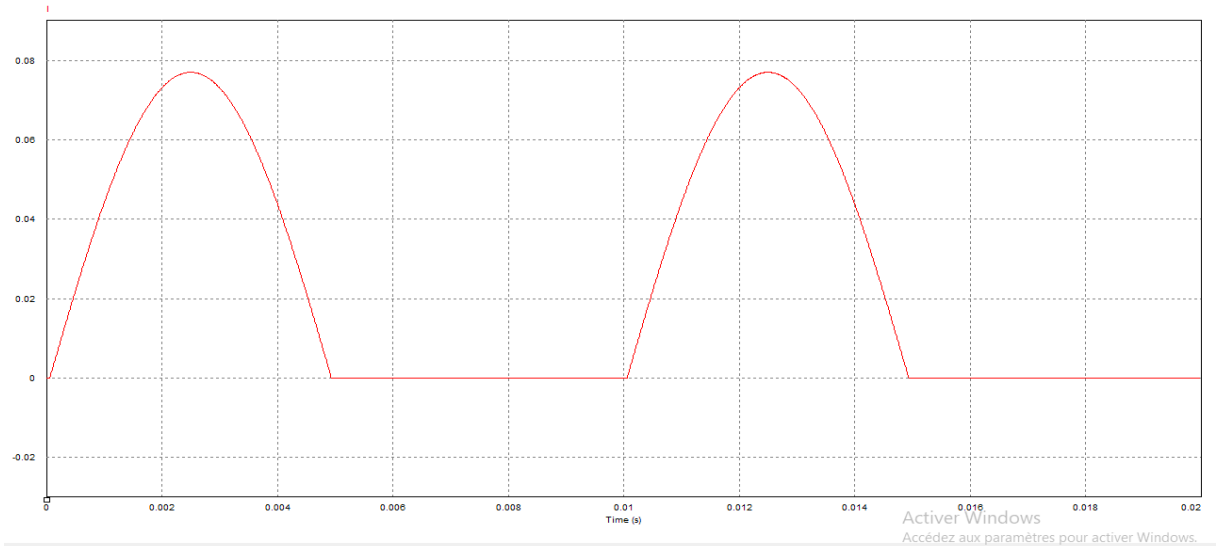

Figure 5 Variation of I_c as a function of time.

<u>Step 2:</u> Full wave rectification (Greatz bridge)

Realize the circuit of Figure 6, with $E_{max} = 8V$ and $f = 100Hz$.

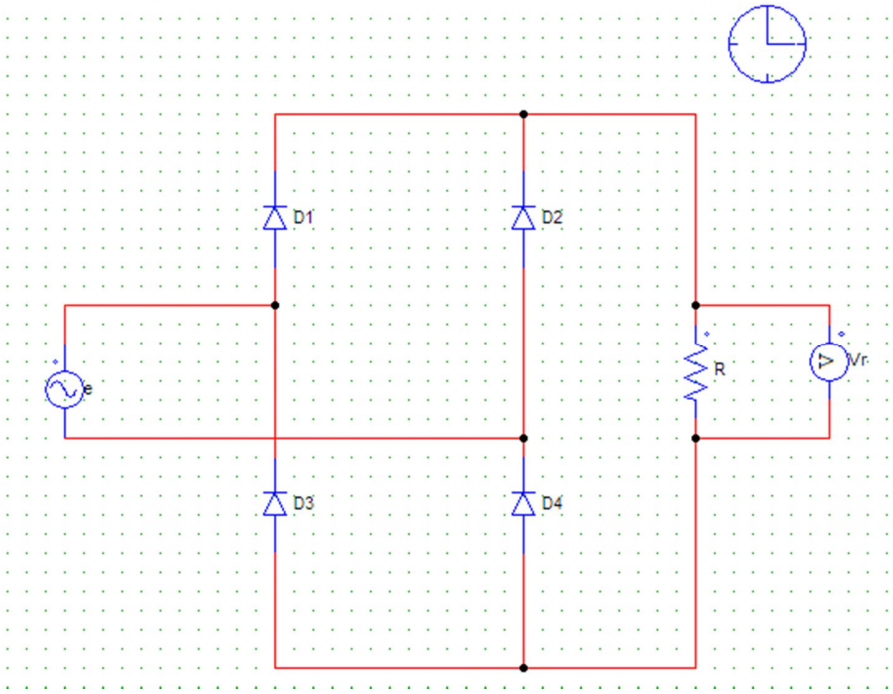

Figure 6 Full wave rectification.

Visualization of the signals $V_R(t)$ is presented in Figure 7.

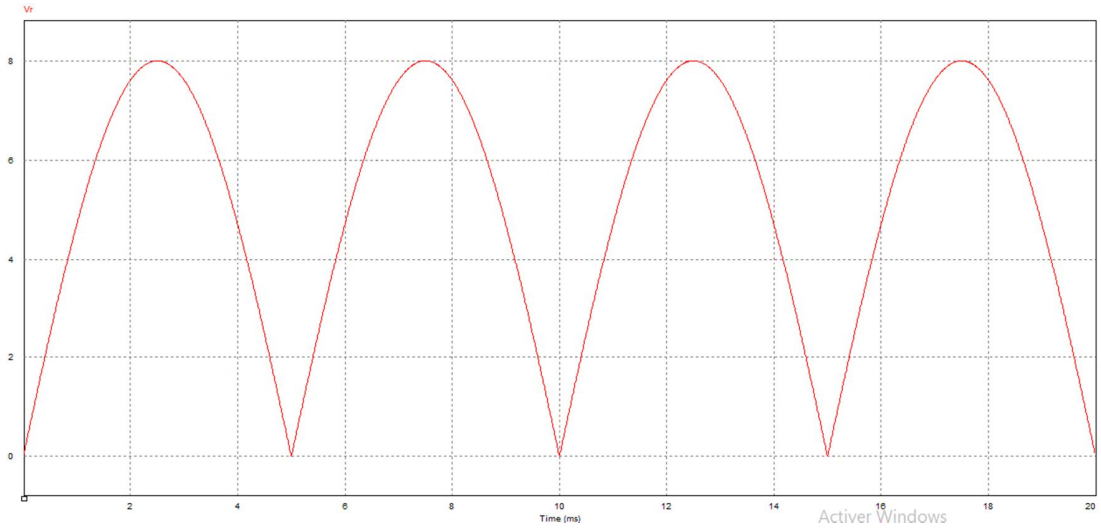

Figure 7 Variation of $V_R(t)$ as a function of time.

The average value of the voltage $V_R(t)$ is: 5.0954755 V. In the case of adding a capacity C parallel with the resistance R (Figure 8).

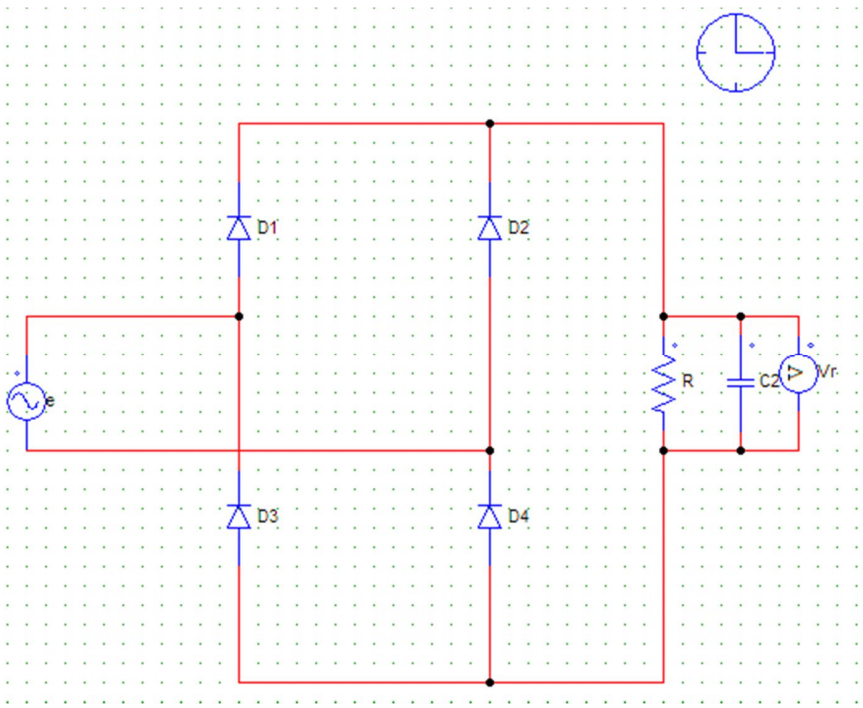

Figure 8 with capacitor C_2= 47µF.

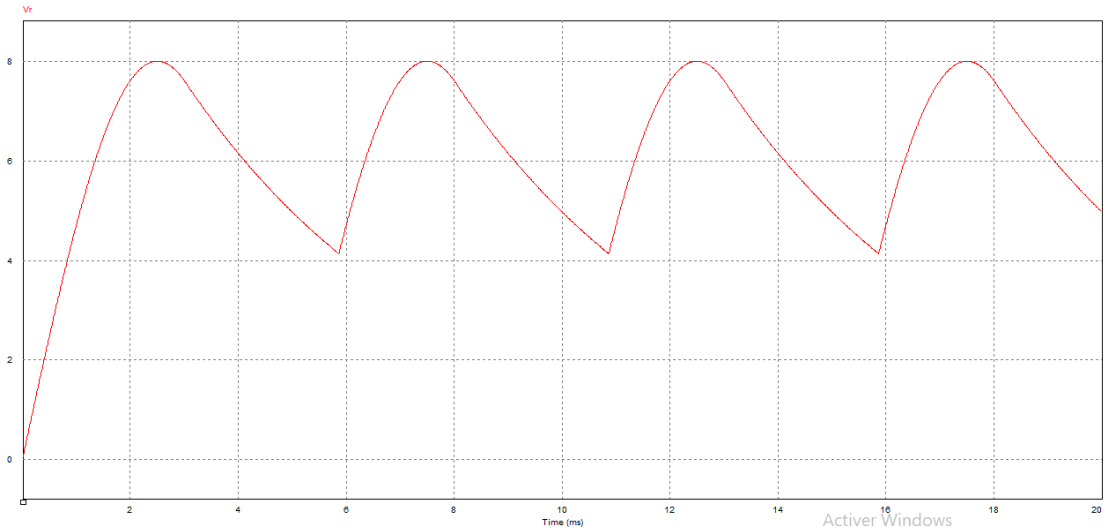

Figure 9 Variation of $V_R(t)$ as a function of time.

The average value of the voltage $V_R(t)$ is : 6.1293726 V.

<u>Step 3:</u> Straightening (filtering)

Realize the circuit of figure 10 , with $E_{max} = 8V$ and $f = 100Hz$.

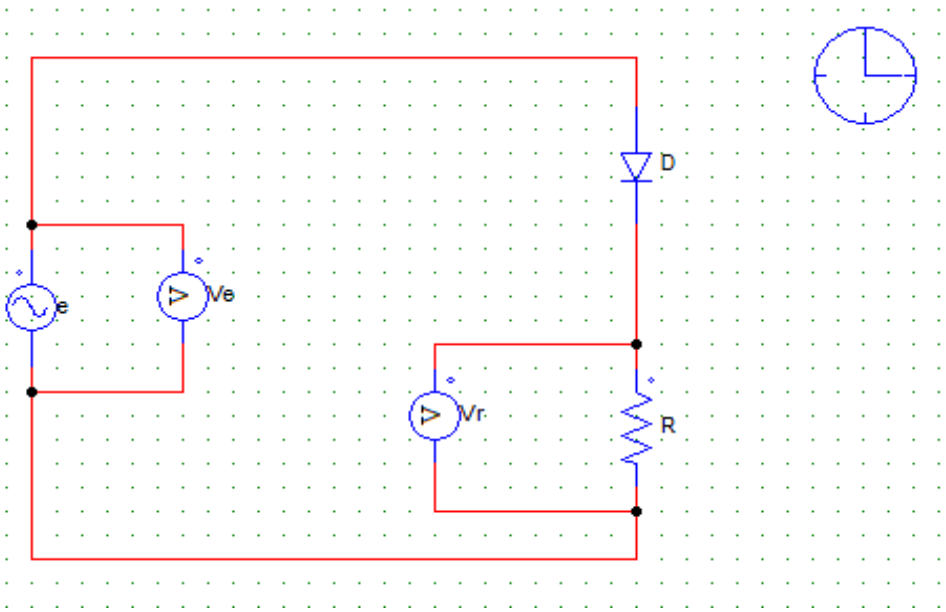

Figure 10 Visualization of the signals e(t) and VR(t).

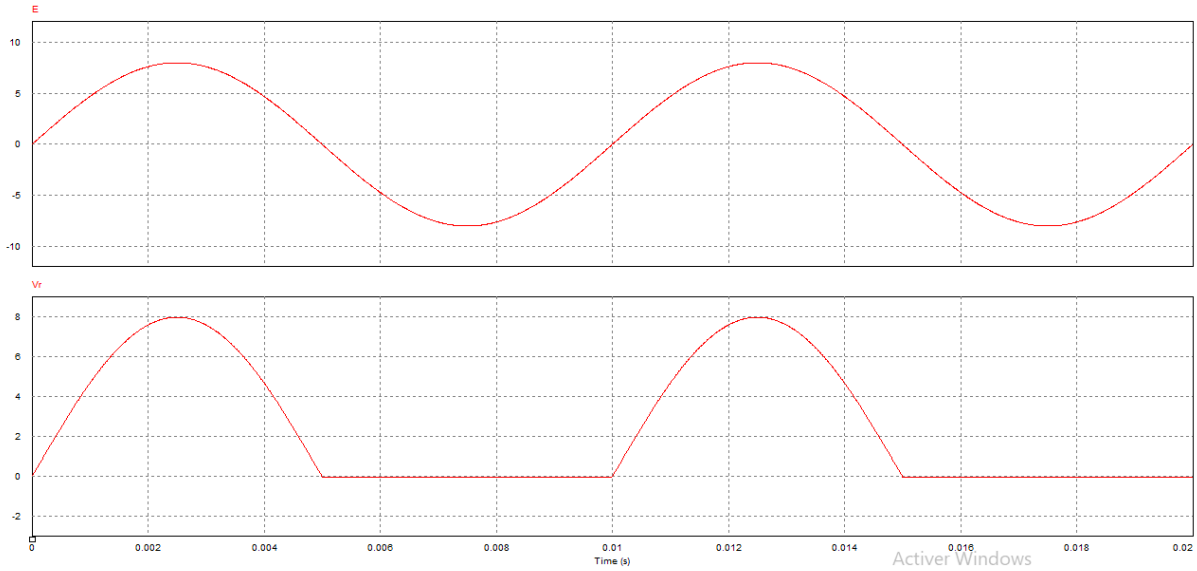

Figure 11 Variation of e(t) and V_R(t) as a function of time.

The average value of the voltage $V_R(t)$ is : 2.5477063 V. If we use capacitors C_1 and C_2 (Figure 12).

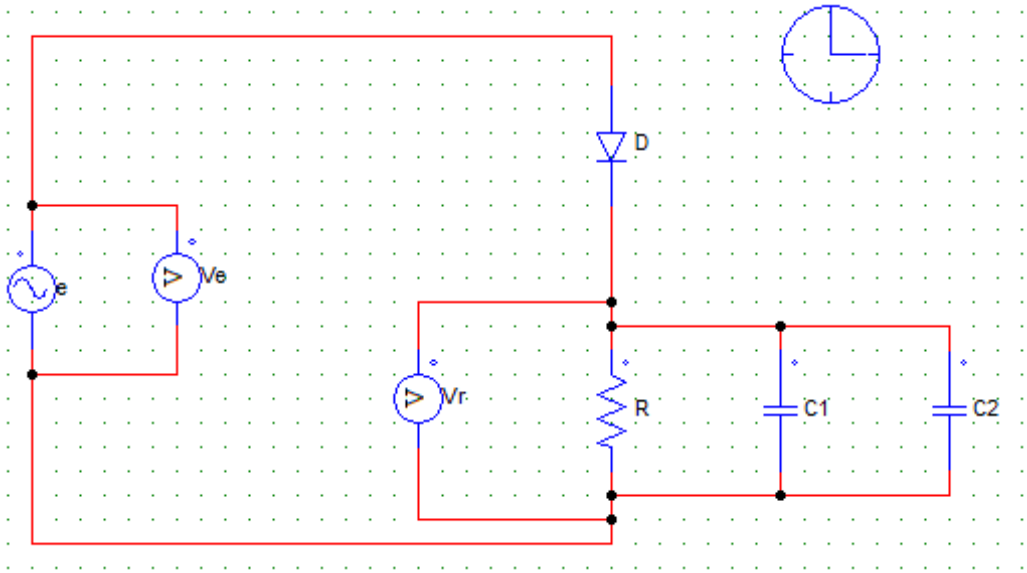

Figure 12 With capacitors C_1 and C_2.

For the capacitor C_1= 10μF, the variation of as V_R(t) a function of time is presented in Figure 13.

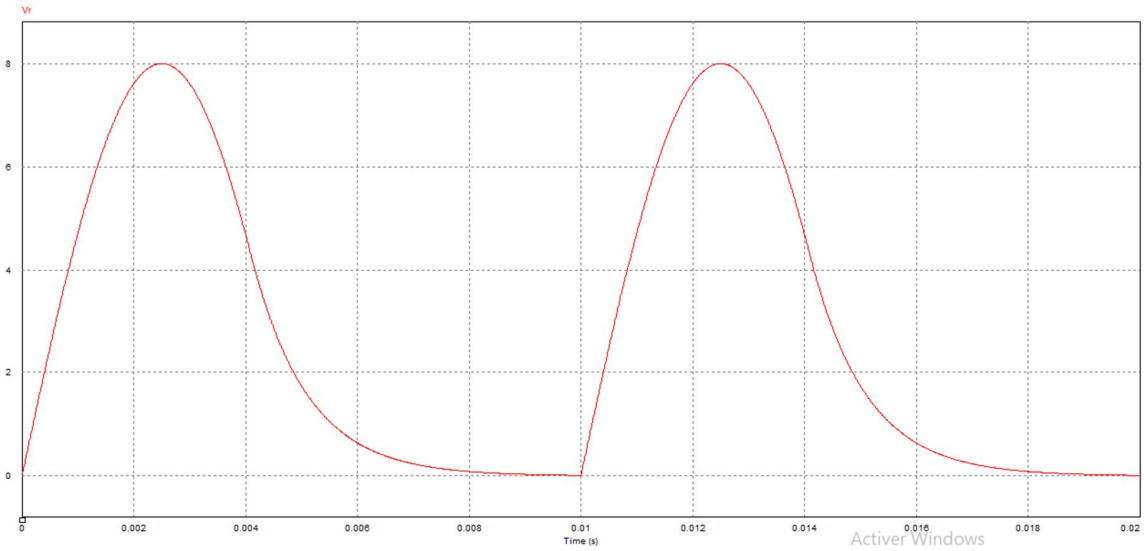

Figure 13 Variation of V_R(t) as a function of time.

The average value of the voltage $V_R(t)$ is: 2.7771290 V.

For the capacitor C_2 = 47μF (Figure 14), the variation of as V_R(t) a function of time is presented in Figure 14.

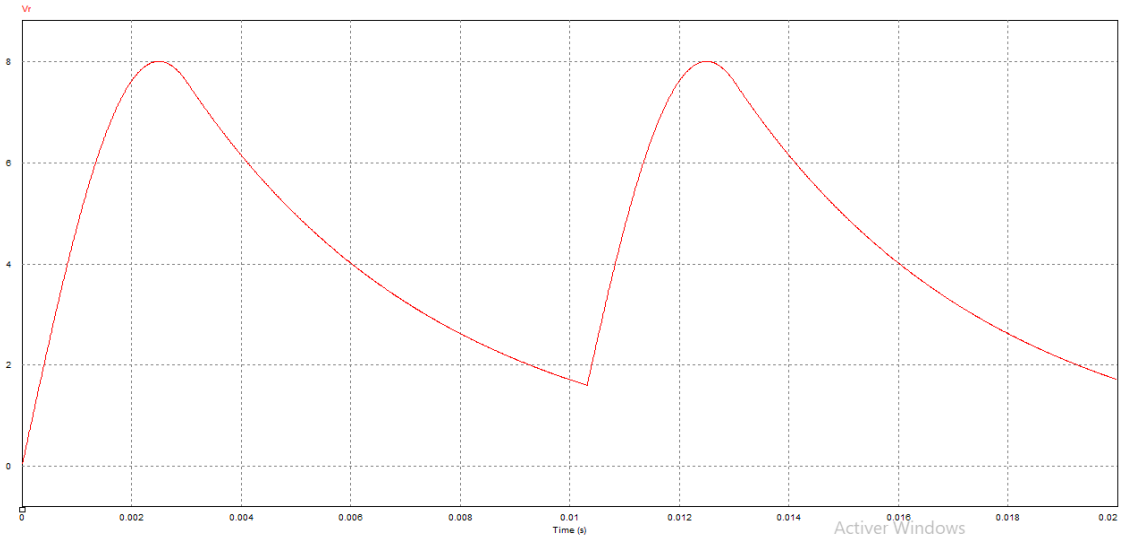

Figure 14 Variation of $V_R(t)$ as a function of time.

The average value of the voltage $V_R(t)$ is: 4.4523665 V.

- **Observation and comparison**

- In the first case the current is sinusoidal in shape.
- In the second case C=10 µF, the discharge path is a little slower until reaching 0, increasing the average voltage up to 2.7771290 V.
- In the third case C = 47µF, the discharge path is slower and does not reach 0, increasing the average voltage up to 4.4523665 V.

Step 4: Zener diode

Realize the circuit of Figure 15, with $E_{max} = 8V$ and $f = 100Hz$. For the Zener select the value of 6 for the 'Break Down Voltage' option and 0.7 for 'Forward Threshold Voltage'.

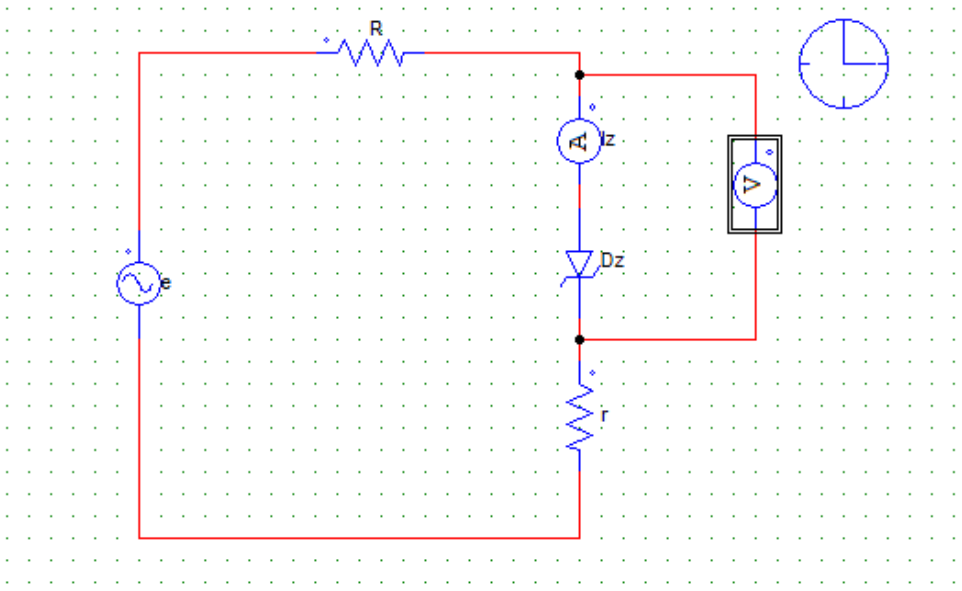

Figure 15 Zener diode circuit.

We visualize the voltage V_Z across the Zener as well as the I_z current flowing through it in Figure 16.

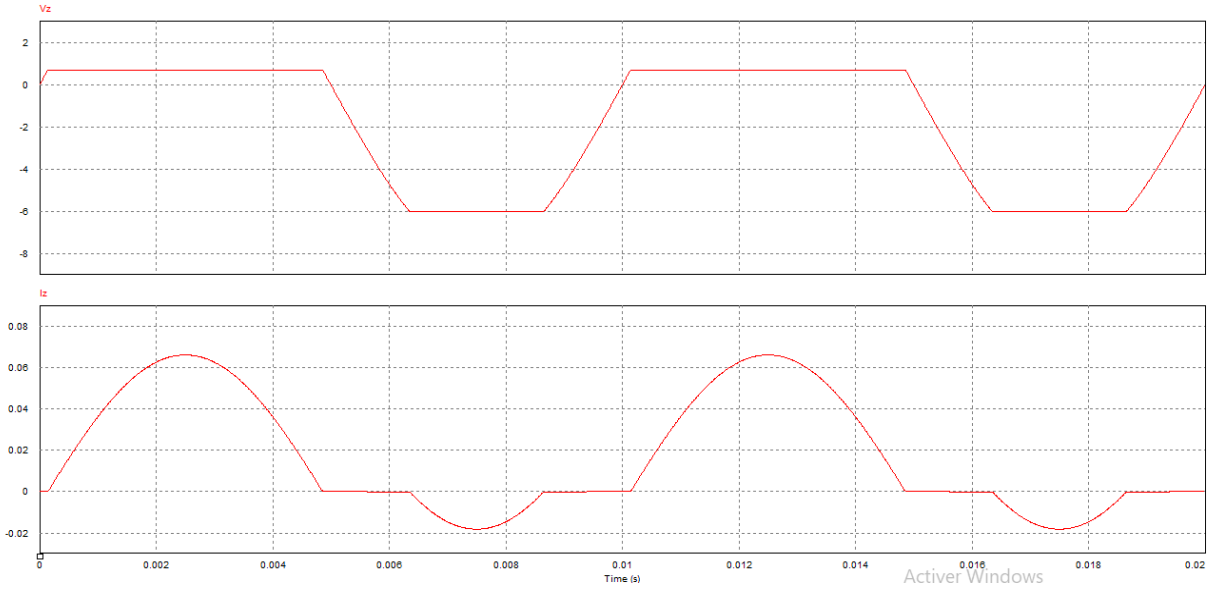

Figure 16 Variation of Vz and Iz as a function of time.

✓ **Justification**

In the positive direction if $v_e(t) > V_s$, the diode becomes conductive therefore $i(t) > 0$ and if $0 < v_e(t) < V_s$, the diode becomes blocked therefore $i(t) = 0$.

In the negative direction if $v_d(t) < V_s < 0$, the diode becomes blocked therefore $i(t) = 0$ and if $v_e(t) < V_d$, the diode becomes conducting therefore $i(t) > 0$.

The variation of I_z as function of V_z is illustrated in Figure 17.

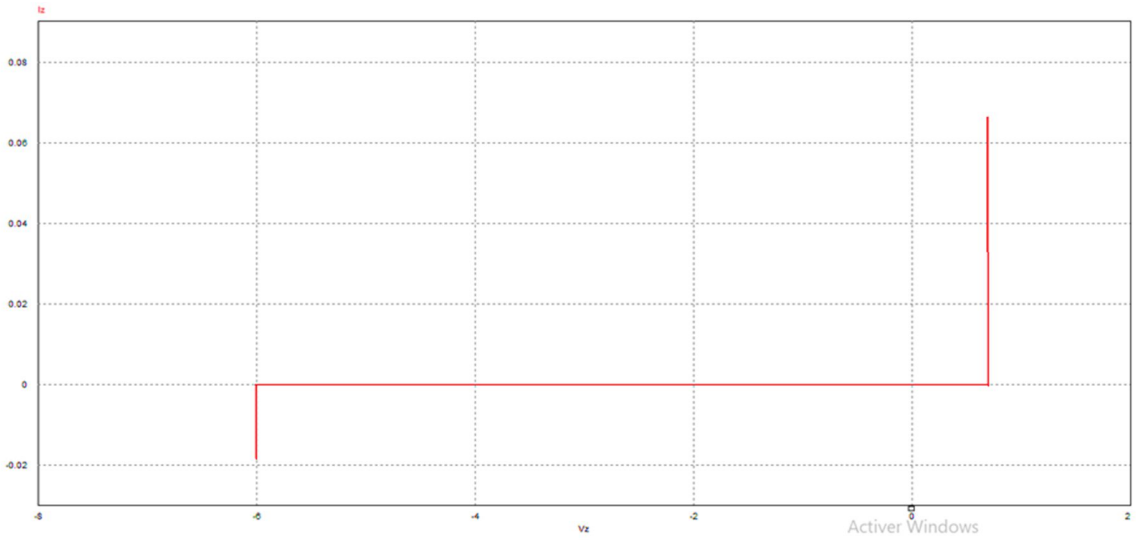

Figure 17 Variation of I_Z as a function of V_z.

5. Analysis of results

In this practical work, we used PSIM simulation software to study the different behaviors of a junction diode (passing - blocked) of a rectifier diode.

Graetz bridge is an assembly of four diodes connected in a bridge which rectifies the sinusoidal current into contained current using a capacitor.

In forward bias the diode behaves like a classic diode with a threshold voltage V_s close to 0.65 V. Beyond the threshold voltage the diode is often modeled by a linear characteristic of slope $1/R_d$.

In reverse bias lower than the Zener voltage, the reverse current is practically zero. Beyond this voltage, the characteristic can be modeled by a steep straight line. In normal use a Zener diode is always used in reverse. It can be modeled by a voltage generator V_z in series with a resistor R_z. The voltage stabilization is all the better as R_z is low. Reverse voltage V_{z0} = - 6 V.

Questions / Discussions:

1) Component that eliminates the fluctuations in rectified voltage and produces relatively smooth DC voltage is:

A filter.

2) The cathode of zener diode in a voltage regulator is normally :

More positive than the anode.

3) When reverse bias is applied to a crystal diode, it :

Raises the potential barrier.

4) For the same a.c. voltage and load impedance, which of the following statements about rectifier are correct?

The average load current in a full wave rectifier is twice than in a half wave rectifier.

The average load current in a full wave rectifier is n times that in a half wave rectifier.

5) For small signal ac operation, a practical forward biased diode can be modeled as :

Resistance

6) What are the three regions in which diodes function?

Forward bias, zero bias and reverse bias are the three regions in which diodes function.

7) Give one application of P-N junction diodes.

P-N junction diodes are used as rectifiers in numerous electric circuits. They are also used as voltage-controlled oscillators in varactors.